Hybrid Transistor for future Power Integrated Circuits

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HYBRID TRANSISTOR FOR FUTURE POWER INTEGRATED CIRCUITS

Master of Science Thesis in
"System on Chip Design (SoC Design)"

by

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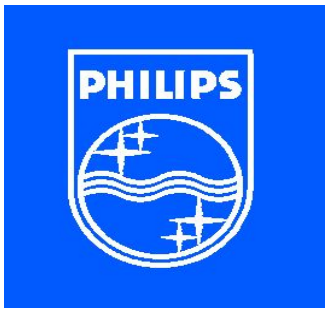

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ABSTRACT

The future Power Integrated Circuits for power management and automotive electronics will require higher level of integration of power electronic components into advanced CMOS technology processes as compared to today's applications. Current generation of lateral high voltage/power devices cannot be further scaled. Given the ever increasing cost per mm^2 of silicon area in every new CMOS generation, the integration of these traditional HV/power components is fast becoming uneconomical. Their replacement with vertical devices, dominating the discrete component market due their inherently better specific on-resistance, which makes them better suitable for scaling, is not obvious. The processing of vertical devices is either incompatible with planar CMOS manufacturing or the integration of both processes results in unacceptably large degree of complexity prohibiting commercialization.

In this work, a novel hybrid transistor combining advantages of both vertical and lateral (planar) devices is analyzed. Similarly to vertical devices, the hybrid transistor features vertical current flow in both gate channel region and drift (or extended-drain) region allowing very low specific on-resistance and thus very compact size. Simultaneously, all device terminals – Source, Drain, Gate and Field Plate – are placed on the top surface, as it is common for planar devices. This fact combined with simple processing guarantees straightforward integration of hybrid transistor into any CMOS technology. The vertical drift region is accompanied with a field plate, which allows high breakdown voltage and low specific on-resistance.

This device was analyzed using numerical simulations. Potential distribution in the off-state was mainly studied with respect to different device parameters, e.g. trench depth and width, doping concentration and oxide thickness under the field plate. We aimed at maximizing breakdown voltage (BV_{DS}) for minimal device size and maximal doping concentration in the drift region. The device construction was optimized for 50 V and 100 V domains.

Finally, the on-state regime of the hybrid power transistor was simulated to determine the specific on-resistance ($R_{on,sp}$). A specific on-resistance of 76.7 $m\Omega mm^2$ for a breakdown voltage of 100 V was determined. This is an excellent $BV_{DS} - R_{on.sp}$ trade-off outperforming any existing lateral device.

Key words: Power Integrated Circuits, Breakdown Voltage, High Voltage, Specific on-resistance, RESURF, Field plate, TrenchMOS, Automotives.

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CHAPTER I INTRODUCTION

1.1 Overview of Power Devices

The power devices play a vital role in current semiconductor technology. Many complex applications require power conversion (say DC-DC conversion). The need for long stand alone operating times and low power consumption when charging the battery, both require the use of efficient power converters. The application use of such high voltage devices can be generally divided into 2 categories; system-in-package (SiP) and system-on-chip (SoC). The SiP combines discrete high voltage components (produced by dedicated technology) with dedicated IC on separate printed boards. The high voltage discrete components are typically vertical devices produced by optimized technology often incompatible with IC processes (such as CMOS process). The SoC represents a solution, where the high voltage transistors are integrated in a silicon chip with the remaining IC components and produced in common IC manufacturing technology as a process option. The device concept under study described in this report targets the SoC solutions and therefore the SiP solutions and corresponding discrete HV device will not be considered.

The integrated power devices have found various applications both in industrial and consumer equipments such as color television, mobile/static displays (cellular phones and portable music players), automotive electronics and telecommunication circuits (see Fig. 1.1). In these applications, the high-voltage transistors are typically used in the following circuits: DC-DC converters, display drivers or power management units. Most of these applications require blocking voltages in sub-200V regime and high current (<10 A) handling capability. The large current capability translates into a relatively large device size (i.e. long transistor width). As the cost per mm^2 of CMOS chip area ever increases, the low specific on-resistance (essentially determining the current handling capability per device area) is absolutely essential.

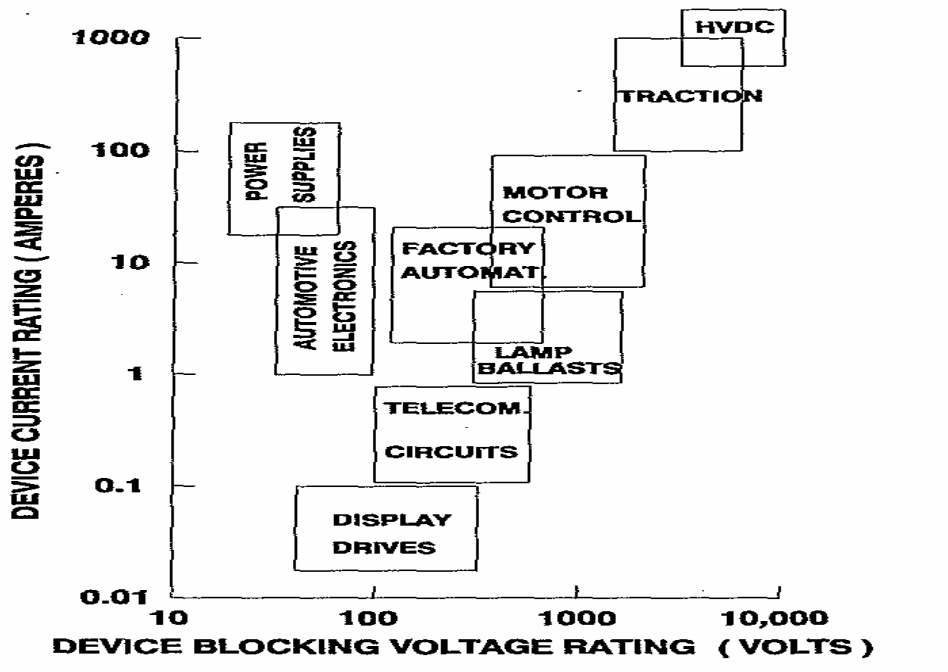

Fig. 1.1: Application of Power devices in relation to voltage and current ratings

1.2 Existing Solutions

Different high voltage options embedded in various CMOS generations have been developed by several semiconductor companies. For example, ABCD (Advanced BiCmos Dmos) of Philips Semiconductors, BCD (BiCmos Dmos) of STMicroelectronics, LBC (Linear BiCmos) of Texas Instrument or SmartMOS offered by Freescale. In all these processes, the high voltage transistors are variants of lateral Double-diffused MOSFET (DMOS), also called extended-drain MOSFET. This type of transistor features a relatively lowly doped drift region separating the drain and gate in order to accommodate the high drain voltage. The gate channel and the drift region both expand in lateral direction (parallel to the silicon wafer surface). As a result the specific on-resistance is relatively large and strongly increases with the breakdown voltage.

To improve the trade-off between breakdown voltage and on-resistance, several Reduced Surface electrical Field (RESURF) methods are employed, e.g. junction RESURF or field plate based RESURF. These methods provides an enhanced depletion in the drift region, which in turn allows higher doping concentration there and thus lower on-resistance without breakdown voltage degradation.

1.3 Studied Device Concept

In this work, a novel power MOSFET, Hybrid MOSFET, is studied. This structure features vertical drift region and vertical gate channel region, which allows maintaining the classical benefits of vertical devices. The breakdown voltage is enhanced by usage of field plate. However, all the device terminals (source, drain, gate and field plate) are located on top surface, which allows straightforward integration with IC processes.

This device construction is thoroughly analyzed with respect to different device parameters. Their influence on the potential distribution inside this novel device is evaluated and the corresponding breakdown voltage is determined. The structure is further optimized for relevant voltage range. These simulations were mainly realized on diodes. At the final stage, the results are verified also on transistors using the previously found optimal parameters. The performance analysis is completed by simulating also the on-state resistance. This allows to establish the breakdown voltage vs. specific on-resistance trade-off and to compare it to existing technologies.

1.5 Structure of the Report

Chapter 1 outlines the background of this work and explains its scientific and industrial relevance.

Chapter 2 describes the simulation tools used in this project.

Chapter 3 discusses a normal 1-dimensional P-N junction diode and the simulated reverse characteristics.

Chapter 4 describes simulation results of field-plated diode and illustrates the influence of the field plate on breakdown voltage.

Chapter 5 introduces the hybrid diode structure. The influence of the different device parameters on its breakdown voltage is demonstrated. The optimization for 50 V and 100 V domains is discussed.

Chapter 6 evaluates the breakdown voltage and on-state characteristics of hybrid transistor (diode with added gate) and compares the achieved breakdown voltage vs. specific on-resistance with existing technologies.

Chapter 7 concludes the work and gives suggestions on the future work followed by abbreviations, symbols, references and appendix.

CHAPTER 2 SIMULATION TOOLS

2.1 INTRODUCTION

The commercially available simulation tools are either process or device simulators with an interface between them to allow device simulations with realistic process impact. These numerical simulators are mainly used for analytical and predictive purposes. They allow rather realistic insight into electronic device without a need to actually manufacture such device. Various physical parameters and phenomena can be analyzed at any location inside the device. This greatly reduces time and cost in semiconductor research and development, and enriches understanding of the device physics.

2.2 MEDICI 2D Device Simulation Program

The MEDICI software is a powerful device simulation program that is used to simulate many electronic devices, including diodes, MOSFETs, JFETs, bipolar transistors etc. This software allows 1-dimensional or 2-dimensional simulations. The simulated device is approximated with a mesh of discrete point emulating the device structure. The doping concentration, type of material and associated material and electrical constants are defined at each mesh points. During the structure definition, the electrodes (locations where voltage and current is applied and/or measured) are also defined. These can be realistic or completely arbitrary allowing a great flexibility in device analysis.

Once the structure definition is completed, an external potential can be applied and the program solves numerically Poisson equation and Continuity equation for electrons and holes. These equations can be solved separately or in combination. It is also possible to operate the device only with a single carrier, e.g. electrons. A number of physical models are incorporated for accurate description of physical phenomena, such as recombination, impact ionization, electrical field as a function of doping and surface scattering etc. Some details about the Medici tool related to our work are shown in the appendix section.

2.3 Simulated Characteristics

In the frame of this thesis report, four devices have been simulated. These are a simple 2D PN-junction (diode), field-plated diode, hybrid diode and hybrid transistor. The reverse characteristics are predominately simulated and breakdown voltage is established. The breakdown voltage is determined by evaluating impact ionization integral and the breakdown voltage is defined as a voltage where this integral reaches unity. These simulations are mainly based on solving Poisson equation only without considering carriers. This is in most cases sufficient and allows reducing substantially the computation time. In some particular structures, the electron and hole carriers are considered to ensure realistic results. This is indicated in the text, wherever appropriate. In case of the simple diode, the reverse current is also simulated, this

again requires carrier inclusion. This is purely to demonstrate the relevance of using the ionization integral for determining the breakdown voltage.

Finally, the hybrid transistor was simulated also in the on-state regime, where also the electron and hole carriers must have been taken into account to calculate the corresponding drain-source current.
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CHAPTER 3 P-N Junction diode

3.1 Introduction

In order to establish the basic understanding of the breakdown voltage in semiconductor devices, a simple p-n junction will be studied initially. This study will be limited to reverse bias regime. A p-n junction diode is formed by combining N-type and P-type semiconductors, as illustrated in Fig. 3.1. The P-type and N-type regions are both homogeneously doped with step junction. The regions with the opposite sides of semiconductor join is usually called metallurgical junction.

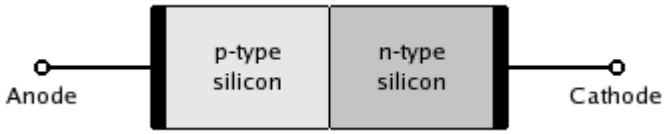

Fig. 3.1: P-N Junction Diode.

In equilibrium state and no applied voltage (V=0V on anode and cathode), the majority carriers in both side of the junction diffuse to its opposite side to distribute uniformly throughout the entire material, i.e. holes from the p-side will diffuse into n-side and electrons from n-side to p-side. This diffusion process leads to charge imbalance (between fixed and mobile charges) on both sides of the junction. This charge imbalance produces an electrical field across the junction, which opposes the diffusion process so that the net flow of carriers is zero in thermal equilibrium. The space charge region, where the mobile carrier concentration is reduced below their thermal equilibrium value is called the depletion region.

The existence of the electrical field across the junction automatically implies existence of electrical potential across the depletion region, even though no external voltage was applied. This potential is called built-in potential and can be considered as similar to the contact potential between two metals.

Under external bias, the potential barrier across the junction either reduces (forward bias regime) or increases (reverse bias regime) so that the current flow exponentially increases with applied voltage in the forward bias regime, while only minute current flows in the reverse bias regime. This small residual current (leakage current) is due to defects and other semiconductor imperfections. A typical I-V curve for a p-n junction is shown in Fig. 3.2.

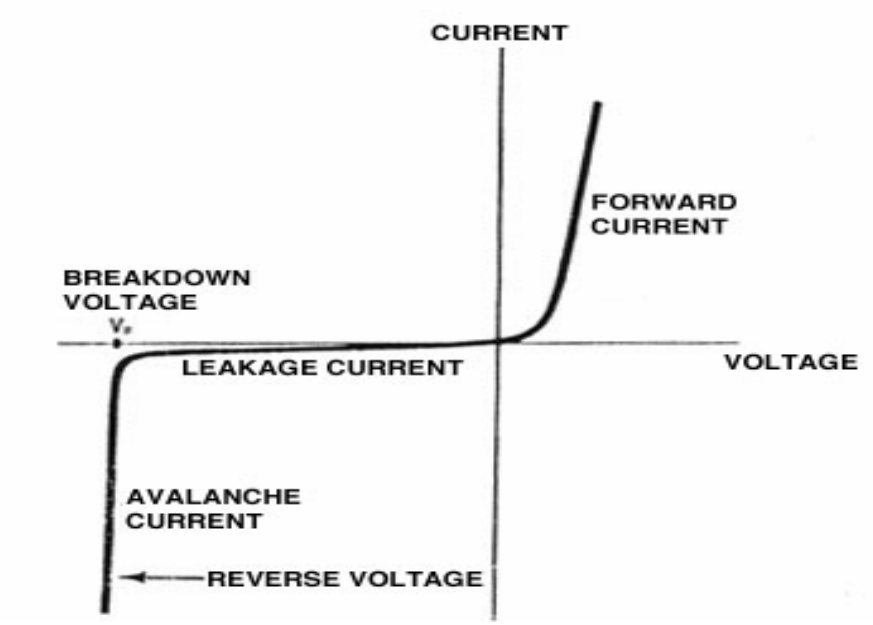

Fig. 3.2: I-V Characteristics of a p-n junction diode.

3.2 Breakdown Voltage

In order to analyze the device breakdown voltage it is necessary to analyze the breakdown characteristics of that device. The maximum reverse bias voltage that can be applied to a p-n diode is limited by breakdown. Breakdown is characterized by the rapid increase of the current under reverse bias. The corresponding applied voltage is referred to as the breakdown voltage showing that the device cannot withstand any further increase in voltage. The cause for breakdown in a device is due to the avalanche effect. The breakdown voltage occurring in a device is inversely proportional to the doping concentration (cm^{-3}). Avalanche breakdown is caused by impact ionization of electron-hole pairs. When applying a high voltage the electric field increases, therefore the carriers gain kinetic energy and generate additional electron-hole pairs through impact ionization.

This process can be quantified through a parameter called the ionization integral. The ionization integral for a one dimensional p-n diode is given by:

$$I = \int_0^W \alpha(E)dx$$

Where x is the spatial coordinate, W the width of the depletion layer, E the electric field and α the ionization coefficient.

Generally, avalanche breakdown occurs when the ionization integral reaches one i.e. unity. If the ionization integral is one then each electron generates another one and this leads to an avalanche breakdown. For this calculation it is enough if only the electric potential is considered and no need of electrons and holes. Therefore the carriers are set to 0 in our calculations.

$$1\text{-}I = 0 \text{ or } I = 1$$

The above formula is for a one dimensional device structure. It shows that every ionization path is directed along a resultant electric field line and all paths yield the same ionization integral. If the electric field in the depletion region is two dimensional, not all ionization paths yield the same ionization integral and every possible path should be considered in calculating the breakdown voltage. The ionization integral first approaching unity determines the onset of breakdown voltage.
The avalanche breakdown voltage of this one dimensional p-n junction diode is characterized by an effective ionization rate α, defined as the average number of ionizing collisions encountered by a hole or electron per unit distance traveled in the field direction. The measurements of the ionization rates of electrons and holes in silicon p-n junction indicate that,

$$\alpha(E) = a.\ exp\ (-b/E) \qquad (1)$$

where a=7.03E5 cm^{-1} and b=1.468E6 Vcm^{-1} for the electric field magnitude 1.75E5 <E<6.4E5 Vcm^{-1} (ref: B.J. Baliga, Power Semiconductor Devices, pg. 67). The average number of ionizing collisions encountered by a single electron/hole crossing the depletion region is given by the ionization integral formula.

The avalanche breakdown voltage for a normal one dimensional p-n junction diode can be approximated using the following formula, (ref. B.J. Baliga, Power Semiconductor Devices, pg. 73)

$$Vbd = 5.34 \times 10^{13}.\ (Na)^{-3/4} \qquad (2)$$

where Vbd is the breakdown voltage and Na is the doping concentration.

This formula was derived under assumption of constant critical electrical field (independent of doping concentration) and depletion is assumed to propagate only in one side of the junction (e.g. N-type is lowly doped, while P-type is very heavily doped).

3.3 The Simulated Structure

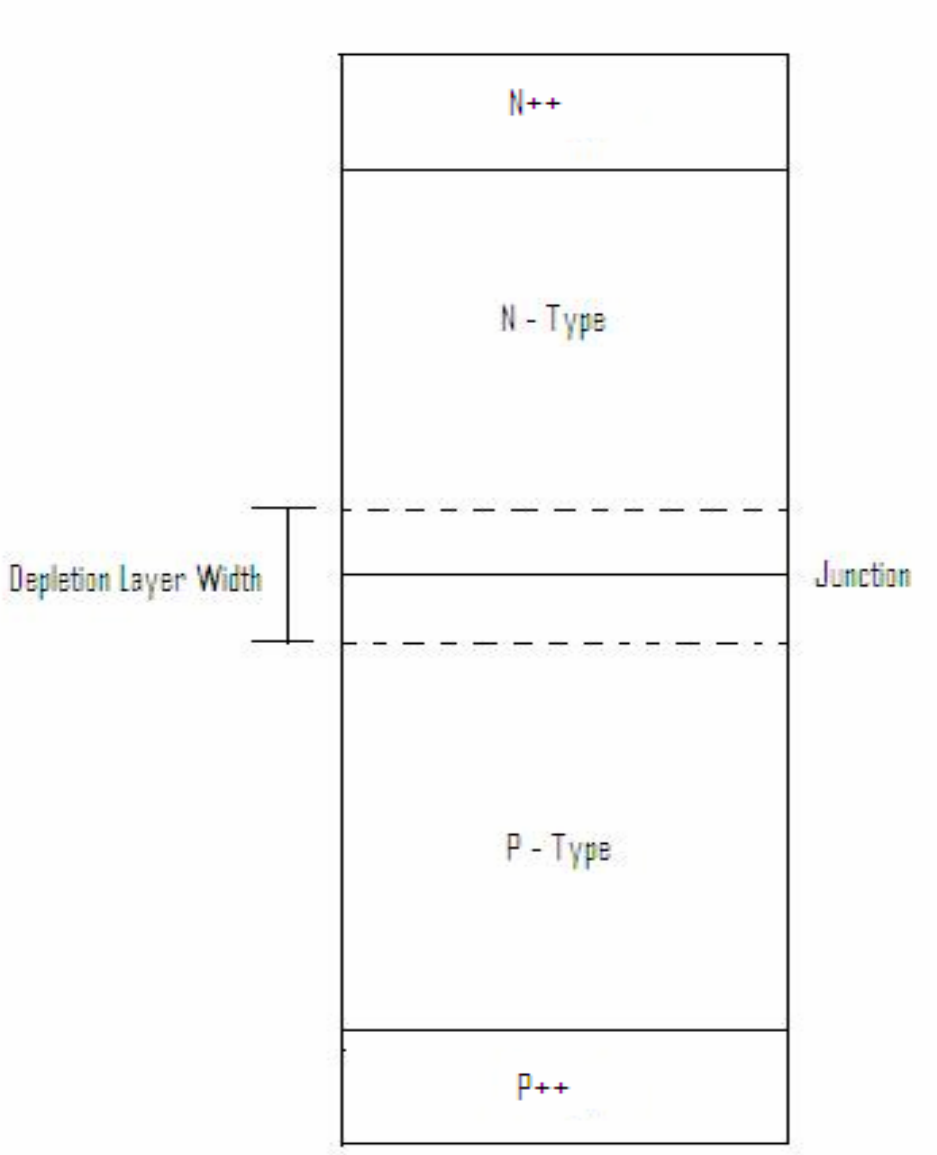

Fig. 3.3: P-N junction diode schematic

The structure shown in Fig. 3.3 is a 2-dimensional P-N junction diode defined within the MEDICI simulation software. It consists of the N-type region (upper part) and P-type (lower part). Heavily doped N++ and P++ regions are established on the outsides of the diode for low ohmic connections. The exact diode parameters using the simulations are given in Table 3.1. The N-type is less doped as compared to P-type side and was designed longer to support the expansion of depletion layer and thus the high voltages. The anode and cathode electrodes are placed on the bottom and top of the device, respectively.

Table 3.1: P-N junction diode parameters

Device Parameters	Values
Device width	2 μm
N-type depth	7.5 μm
N++ width	1.15 μm
P-type width	5 μm
P++ width	1.15 μm
N- region doping (N-)	1E17 cm^{-3}
N++ region doping (N++)	1E20 cm^{-3}
P- region doping (P-)	2E17 cm^{-3}
P++ region doping (P++)	1E20 cm^{-3}

3.4 Simulation and Analysis

The 2-dimensional P-N junction diode was simulated with the above parameters and analyzed for different doping values. In this studied structure the doping concentration on one side of the junction is large when compared to the other side. For example the P region is doped more than the N- region. Therefore the depletion region extends primarily on the lightly doped side of the junction (N- region). This is illustrated in Fig. 3.4, where the carrier concentrations near the metallurgical junction are compared for zero volt bias and small reverse bias. As one can see, a larger portion of the N-type region is free of electrons.

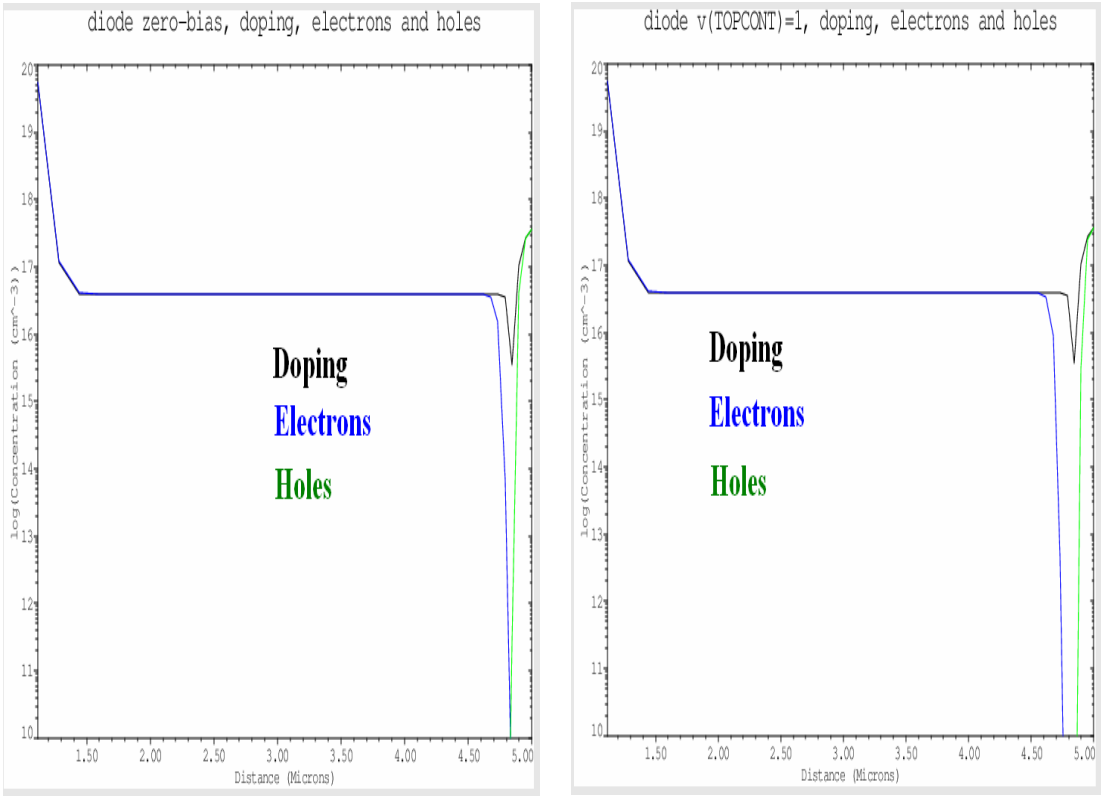

Fig. 3.4: Doping, Electron and Hole concentration at zero bias (left) and reverse voltage of 1V (right).

According to Eq.2, the breakdown voltage depends on the doping concentration in the less doped side of the junction. From the device simulation it is clear that the depletion region width is larger for junctions with lower doping concentration on the lightly doped side (see Fig. 3.5). The breakdown voltage was also determined for different doping concentrations as shown in Fig. 3.6. As an example, for a breakdown voltage of 80V, it is necessary to use a doping concentration for the lightly doped region of 6E15 cm^{-3}.

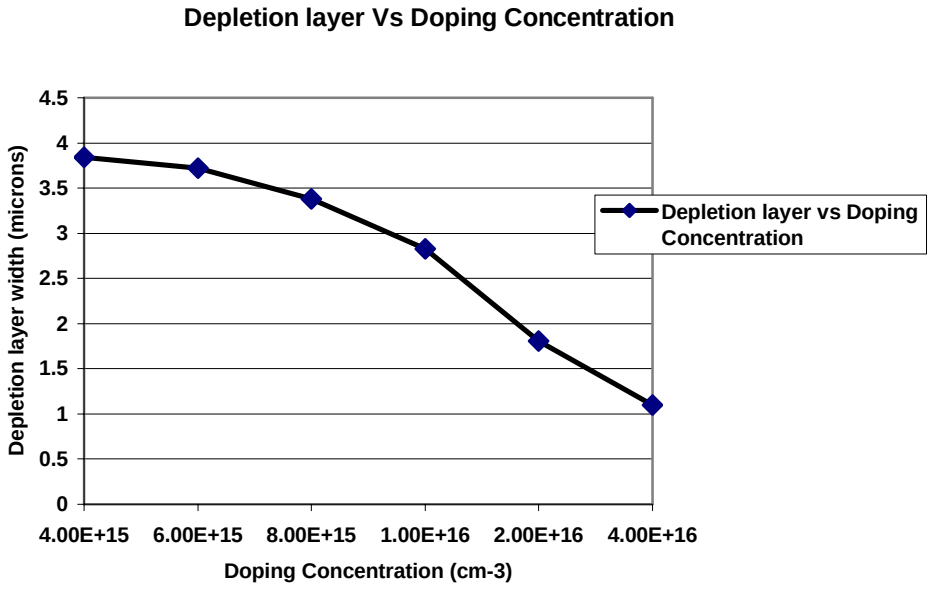

Fig. 3.5: Depletion layer width as a function of doping concentration

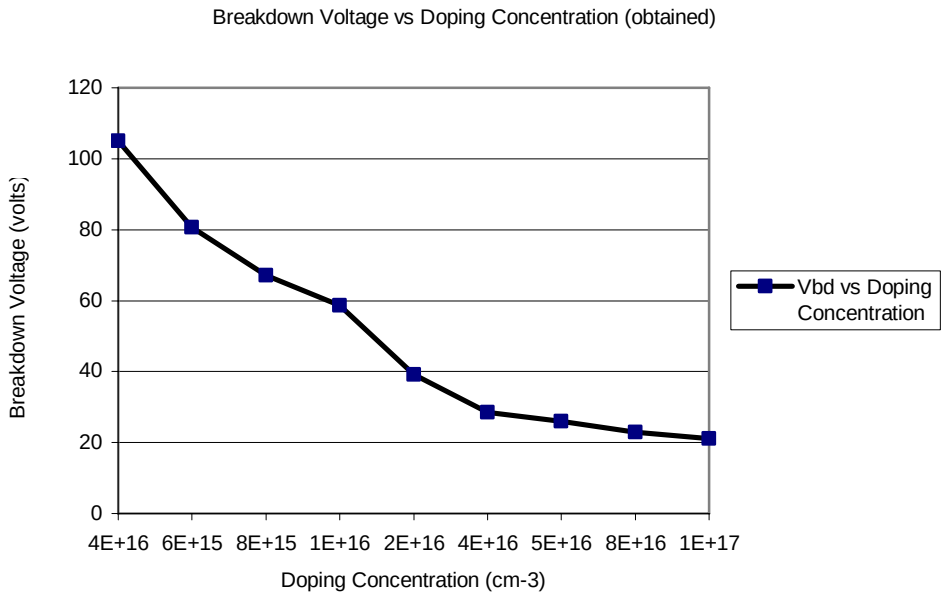

Fig. 3.6: Simulated Breakdown voltage vs. Doping concentration

The previously discussed simulations were performed by solving only Poisson equation. In order to demonstrate the I-V characteristics in the reverse bias regime, further simulations were done assuming also electrons and holes. An example of such I-V characteristics is shown in Fig. 3.7.

The P++ region is connected to the negative terminal and the N++ type region to the positive terminal which therefore produces the reverse-bias effect. As the P-type region is now connected to the negative terminal of the power supply, the holes in the P-type region are pulled away from the junction, causing the width of the non conducting depletion zone to increase. Similarly, the N-type region is connected to the positive terminal; the electrons will also be pulled away from the junction. This effectively increases the potential barrier and greatly increases the resistance against the flow of charge carriers. Therefore there will be no current across the junction or crossing over the junction. At the middle of the junction of the p-n material, a depletion region is created to withstand the reverse voltage. But the width of this depletion region grows larger with increase in voltage. The electric field also increases as the reverse voltage increases. When the electric field increases beyond a critical level, the junction breaks down and current begins to flow due to avalanche breakdown. In this particular case, a breakdown voltage of approximately 25V is observed with a steep increase in current beyond this reverse voltage. Once a very large current is achieved, the current saturates again. This effect is associated with high-injection level and will not be discussed here.

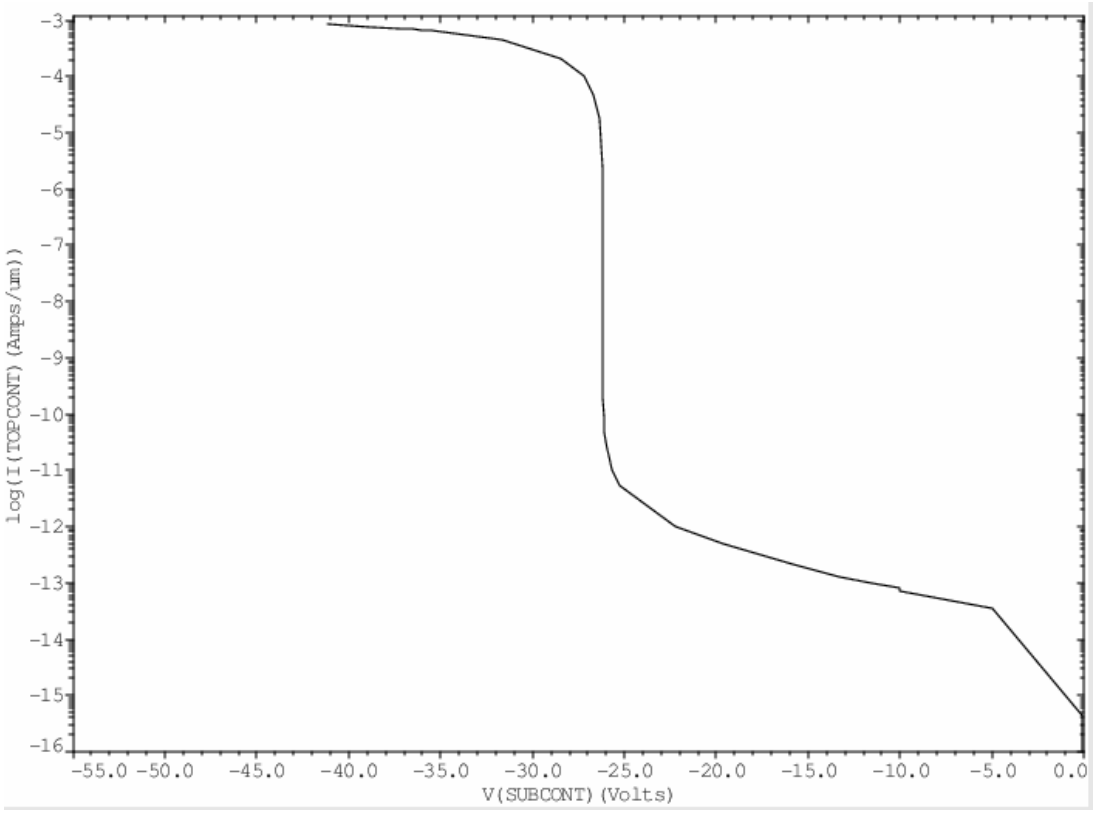

Fig. 3.7: Reverse Characteristic

3.5 Analytical vs Numerical results

In order to verify the simulated breakdown voltage values, we have compared them with values calculated using the analytical Eq.2. This comparison is shown in Fig. 3.8. The simulated data corresponds well with the analytical calculations. There is a small discrepancy at higher doping concentrations; here the simulated breakdown voltage is larger than the calculated values. This is due to the depletion layer in the P-side of the junction that is not taken into account in the analytical calculation, but it is present during simulation.

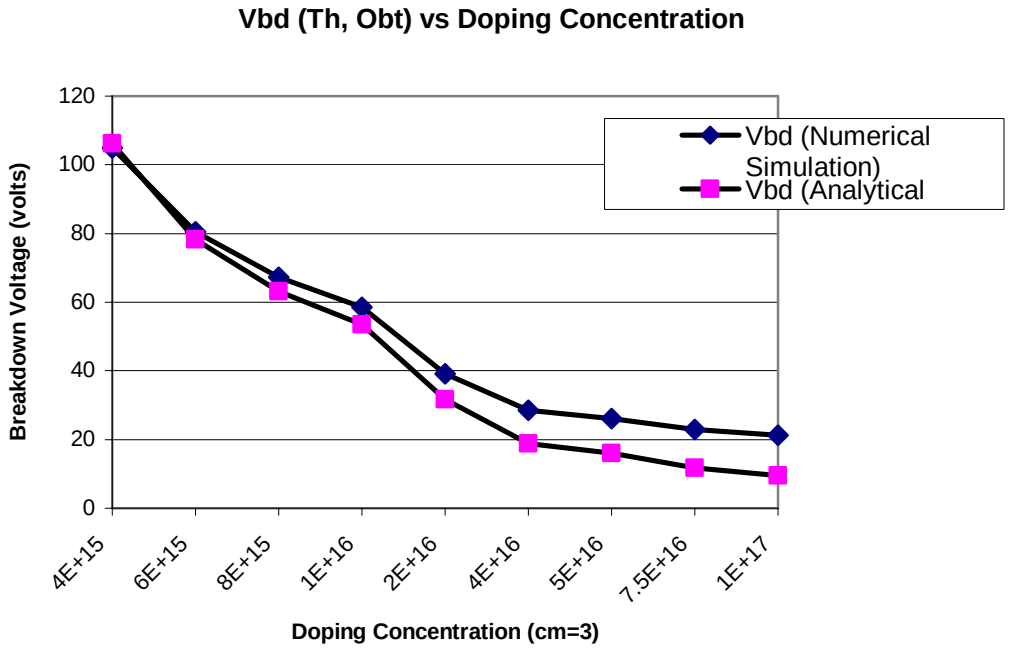

Fig. 3.8: Breakdown voltage as a function of doping concentration: numerical simulation vs. analytical calculation.

CHAPTER 4 FIELD-PLATED DIODE

4.1 Field Plate and Breakdown Voltage

In this chapter a concept of vertical diode with a field plate located in deep trench is described. The field plate is a conductive electrode placed in parallel with the drift region and insulated by a thick oxide layer from the drift region. The field plate is biased at zero voltage during the device operation. The grounded electrode is capacitively coupled to the drift region through the thick oxide. This results in depletion of the drift region near the interface with the oxide. This additional depletion layer joins with the depletion layer formed around the metallurgical junction of the diode. If the full length of the drift region is depleted (by the combined depletion layers), the total reverse voltage is distributed across the entire drift region length. This is typically much longer than the junction depletion width only. In a well designed device, a 20 V per micron of drift length can be supported. It is essential that the full depletion of the drift region must be achieved before the peak electrical field at the junction reaches the critical value.

The extra depletion layer due to the field plate action depends on several parameters; the drift region doping, the drift region width and the thick oxide layer thickness. The optimal doping concentration in the drift region can be calculated using the following equation,

$$\mathrm{N(x)} = \frac{V}{W} \times \frac{\in o \in si}{qTs} \times \frac{1}{(Ts/2 + ((\in si / \in ox).Tox))}, \qquad (3)$$

where V is the applied voltage, W the depletion layer width, Tox the oxide thickness and Ts the silicon width.

This chapter discusses numerical simulations performed with the field-plated diode varying the key parameters governing the breakdown voltage enhancement. As the hybrid diode/transistor employs the field plate, this provides basis for the hybrid device simulations.

4.2 The simulated Structure

The field-plated diode structure shown in Fig. 4.1 is modeled with the device simulator MEDICI. This device has the basic structure of an ordinary P-N junction diode with highly doped P++ region on the top surface and moderately doped P-region with the lowly doped N-drift region below. The highly doped N++ region is at the bottom of the structure. The device differs from the previous by a field plate placed in a trench manner extending along the drift region and separated from it by a thick oxide (i.e. insulating layer). Since the lateral devices occupy more area, a vertical like structure is preferred. In order to obtain optimum field plate effect the device was simulated by altering the doping concentrations and oxide thickness and their breakdown voltage values were determined.

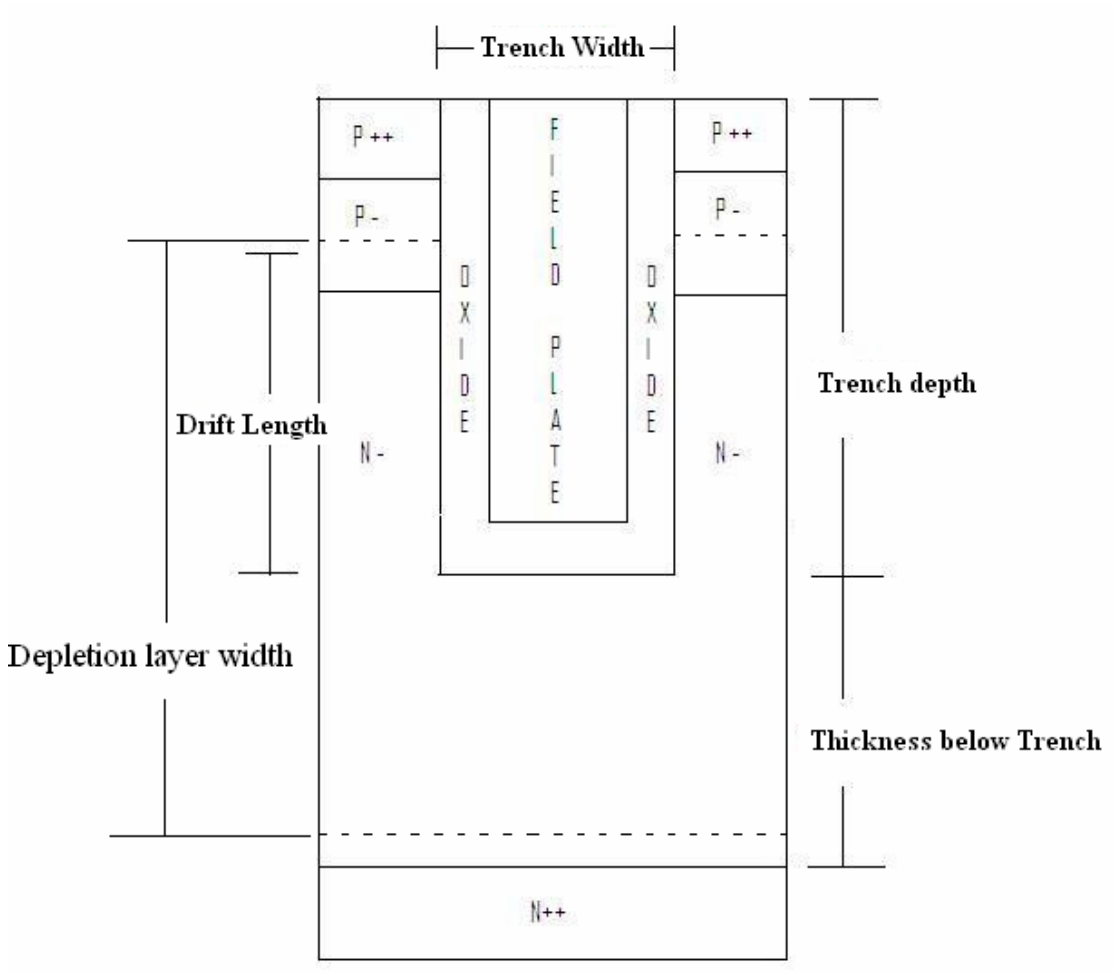

Fig. 4.1: Schematic of field-plated diode.

Table 4.1: Parameters used for simulation of the field-plated diode.

Device Parameters	Values
Trench Depth	4 μm
Drift Region length	3 μm
Trench Width	5 μm
Actual Width	1 μm
Thickness below Trench	0.25 μm
N- drift region doping	8E15, 1E16, 2E16, 5E16, 1E17 cm^{-3}
P- body doping	1E18 cm^{-3}
Tox	0.1 – 1.0 μm

4.3 Simulation and Analysis

The key function of this RESURF technology is it enhances the depletion layer therefore obtaining a higher breakdown voltage. In order to optimize this RESURF effect the thickness of the oxide layer (Tox) and the drift region impurity concentration (Ndrift) are varied. The other important parameters are the drift region length and thickness below trench.

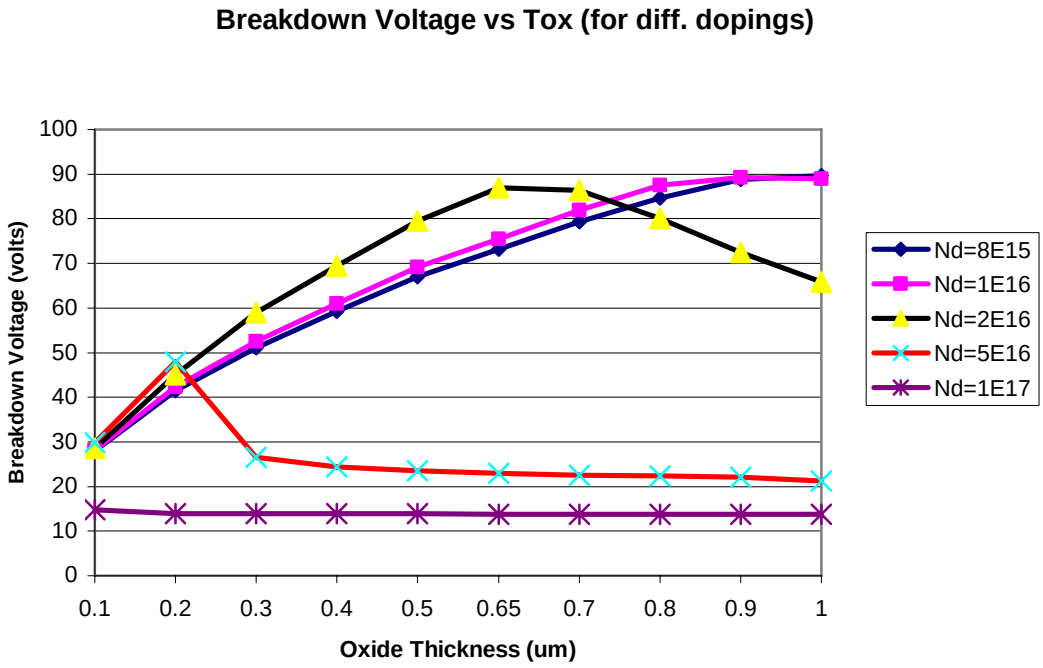

Fig. 4.2: Breakdown voltage vs. Oxide thickness.

Fig. 4.2 shows the simulated breakdown voltage as a function of oxide thickness for different values of drift region doping. It clearly illustrates an optimum in oxide thickness to reach maximal breakdown voltage. For Tox smaller than optimum, the breakdown voltage is limited by the potential sustainable across this oxide layer. For Tox larger than optimum, the capacitive coupling is too weak to deplete the full drift region. There is also an optimal doping concentration of the drift region. Ndrift larger than optimal prohibit full depletion of the drift region before critical electrical field is reached.

This is further illustrated by plotting the potential and electrical field map inside the device. In case of an optimal field-plated device (see Fig. 4.3), the complete drift region is depleted (the depletion is seen by the dotted line), the equipotential lines are uniformly distributed and a constant electrical field is obtained along the drift region. In case of non-optimal field-plate device (too large doping, see Fig. 4.4), the drift region is not completely depleted before critical electrical field is reached and an early breakdown voltage is observed.

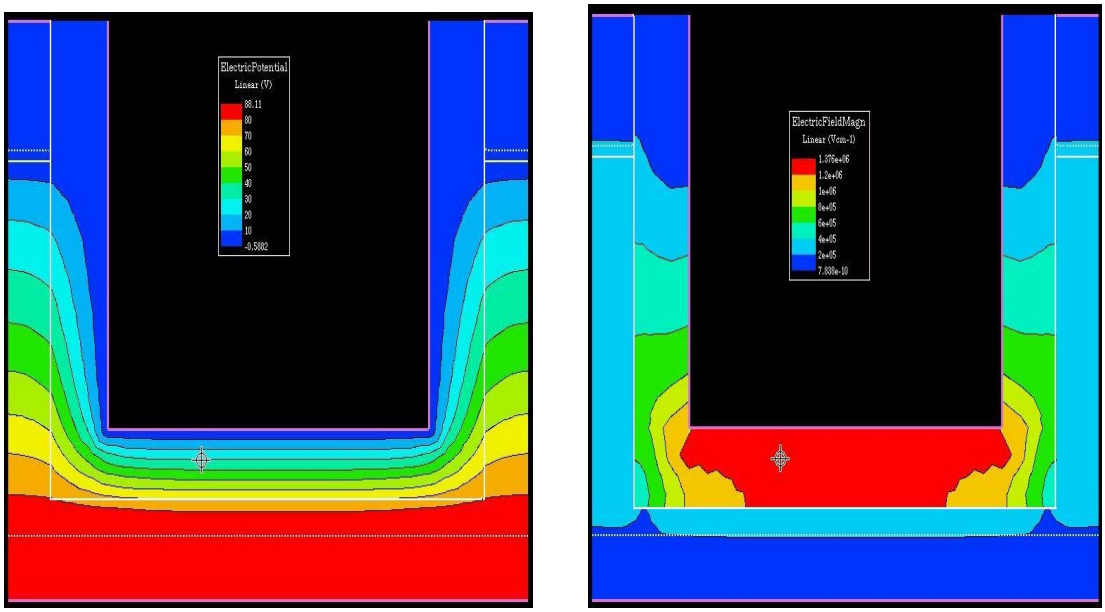

Fig. 4.3: Potential distribution (left) and electrical field distribution (right) for an optimal design of field-plated diode; Ndrift=2E16 cm^{-3}, Tox=0.65 microns.

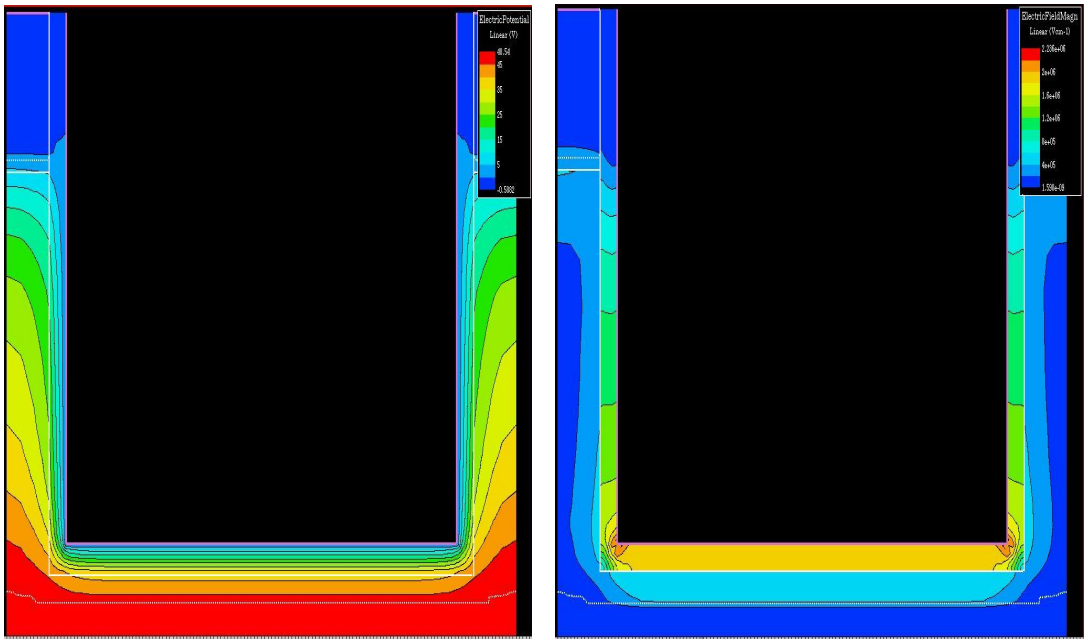

Fig. 4.4: Potential distribution (left) and electrical field distribution (right) for non-optimal design of field-plated diode; Ndrift=5E16 cm^{-3}, Tox=0.2 microns.

As discussed earlier, the drift length also has an impact in the breakdown voltage. The device was simulated by altering the drift length and keeping all other parameters constant. The simulation results show that by increasing the drift length the breakdown voltage also is increased (see Fig. 4.5).

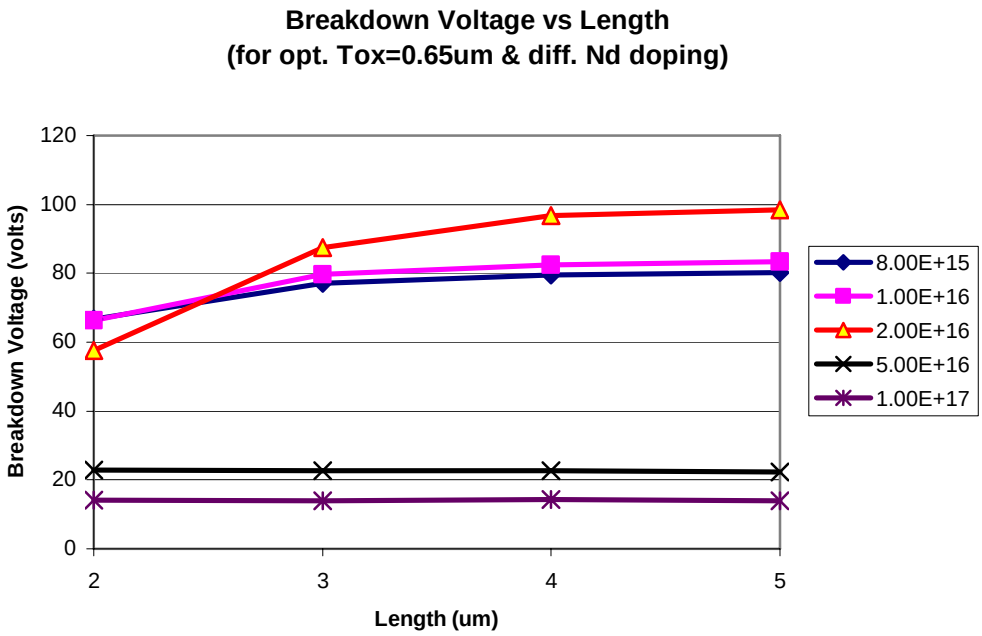

Fig. 4.5: Breakdown voltage vs. drift length.

4.4 Normal diode vs. Field-Plated diode

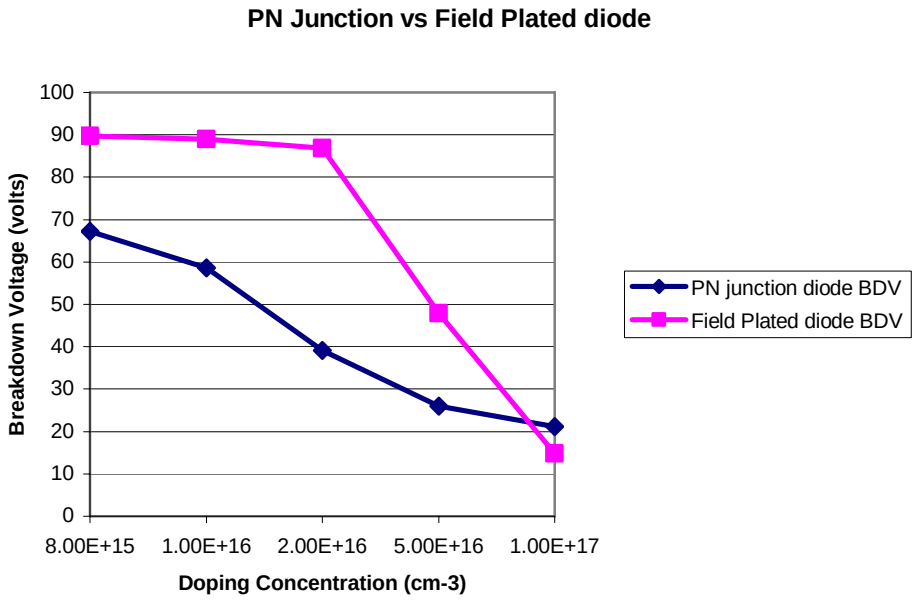

Fig. 4.6: Comparison graph between P-N junction and field-plated diode breakdown voltages for various doping concentrations.

From the above figure it is clear that we have obtained a higher breakdown voltage in the field-plated diode using RESURF concept than the normal diode.

It has been shown that device with optimal parameters can withstand a maximum voltage of 87 V for a doping concentration of 2E16 and 0.65 μm oxide thickness.

CHAPTER 5 HYBRID DIODE

5.1 Hybrid high voltage device: Introduction

In this chapter a hybrid diode vertical in structure with the field plate effect is discussed. The hybrid device feature again a field plate located in deep trench and insulated from the drift region by a thick oxide layer. Differently from the classical vertical field-plated device (see Chapter 4), the drain is located on top surface and the drift region stretches along the trench. So that the current flows downwards, under the trench and upwards again along the trench sidewalls, where it enters the vertical gate channel. This full vertical current flow is expected to yield a transistor with high voltage capability and very compact size.

In order to study the blocking voltage capability of the hybrid device, it is sufficient to investigate a hybrid diode, which is essentially identical to hybrid transistor, but does not include gate. The device was simulated for various parametric values. It was finally optimized to obtain breakdown voltages up to 50V and 100V.

5.2 The Simulated Structure

The hybrid diode has a similar structure like the previous vertical diode with field plate placed in a trench manner. Here the N++ region is at the top (right) with N- drift region stretching along the field plate. The P++ region and medium doped P body region are located at the top (left) remains the same as in the classical field-plated diode. The lowly doped P- substrate is at the bottom of the device structure and is connected to ground via a bottom electrode. Table 5.1 lists the parameters that were varied in the simulations. It also gives their range used to optimize the voltage blocking capability.

Table 5.1: Hybrid diode; simulation parameters and their range.

Hybrid diode parameters	Range of values
Trench width	0.8 - 5 μm
Trench depth	0.95 - 5 μm
Actual width	1 μm
Thickness below trench	0.1- 0.9 μm
N- drift region doping	1E14 – 1E17 cm^{-3}
P- (body depth) doping	1E18 cm^{-3}
P substrate doping	3E15 cm^{-3}
Tox	0.05 – 0.48 μm
Drift length	3-14 μm

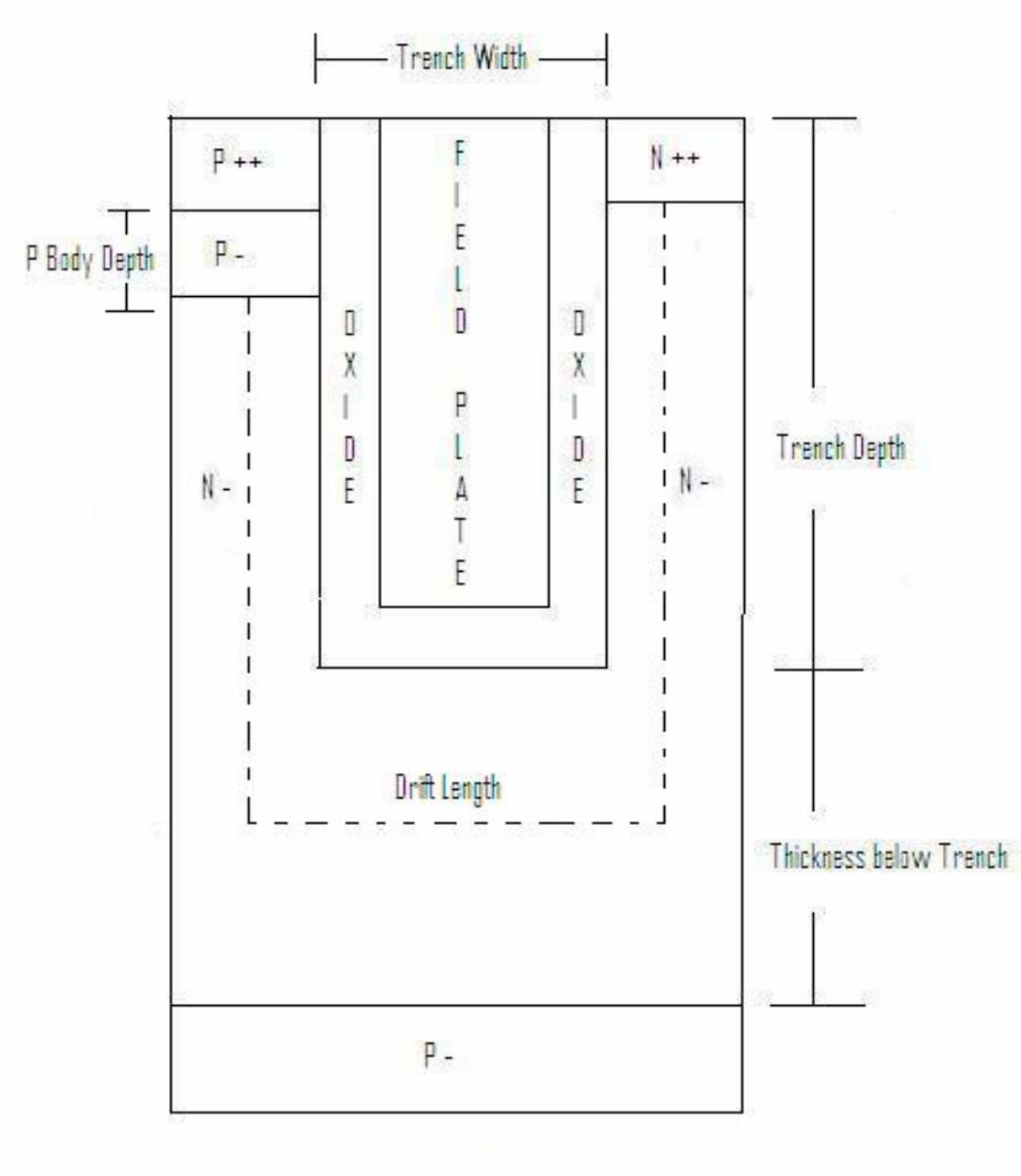

Fig. 5.1: Hybrid diode schematic.

5.3 Simulation and Analysis:

In this section the hybrid diode device simulated by altering the device parameters for different doping concentrations, oxide thicknesses, trench width and trench depth will be discussed in detail. The device was simulated varying oxide thickness (Tox) and drift region doping concentration (N drift). Other parameters were kept constant. In most cases, it was sufficient to solve only Poisson equation without using carriers. For high doping concentration of the drift region (N drift >= 5e16 cm^{-3}), the particular structure construction leads to floating islands surrounded by fully depleted regions. In such case, the simulation included also continuity equations for electrons and holes to guarantee correct results.

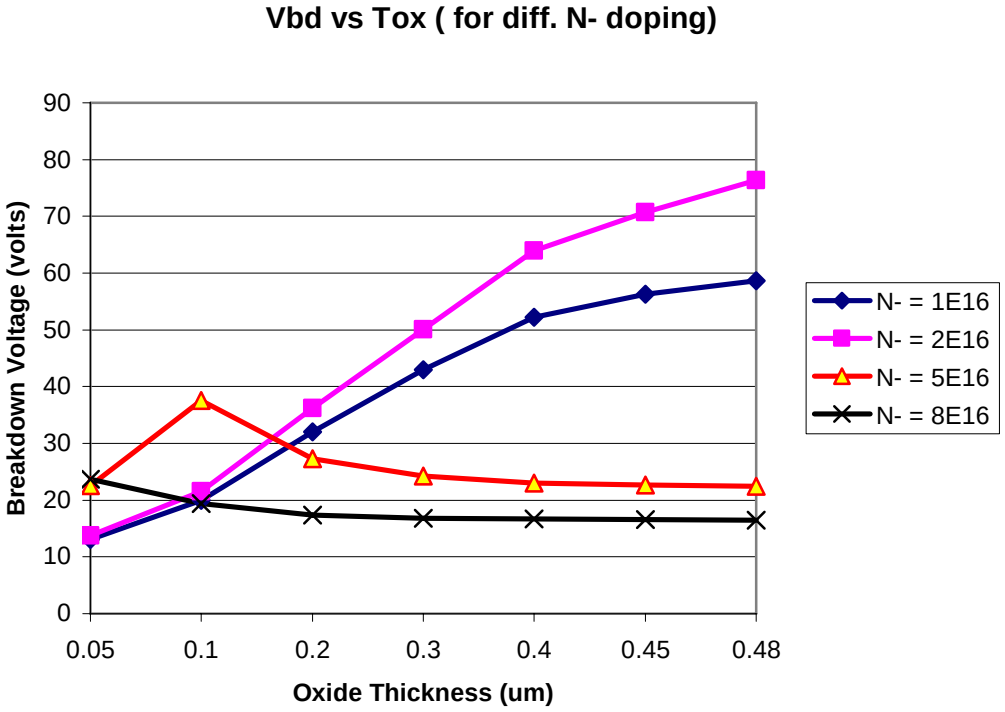

Fig. 5.2: Breakdown voltage vs. Oxide thickness.

The breakdown voltage as a function of Tox and Ndrift is shown in Fig. 5.2. As one can see, the Ndrift = 2e16 cm^{-3} is an optimal value for the drift region doping and there is an optimal oxide thickness leading to the highest breakdown voltage. For better understanding of mechanisms responsible for the breakdown voltage at different design parameters, we have studied the potential and electrical field distribution inside the hybrid diode.

For Ndrift = 2e16 cm^{-3} (see Fig. 5.3), one can see that the full drift region is depleted for Tox = 0.1 microns as well as for Tox = 0.48 microns. The potential is distributed almost linearly on both sides of the trench as well as underneath the trench, which is very good. The electrical field distribution indicates that the critical electrical field is reached under the drain (top right corner of the device) near the interface with the thick oxide. This is because the thick oxide has to withstand the full voltage between drain (on high voltage) and field plate (zero voltage). The oxide itself is sufficiently thick to withstand such voltage difference, but due to the permittivity difference between oxide and silicon, the electrical field in silicon at the interface exceeds the

critical value. Clearly, further increase in oxide thickness will reduce this bottleneck and even higher breakdown voltage will be achieved. However, the field plate effect reduces with a thicker oxide. Once the oxide thickness exceeds optimal value, the breakdown voltage will decrease again due to loss of the field plate coupling.

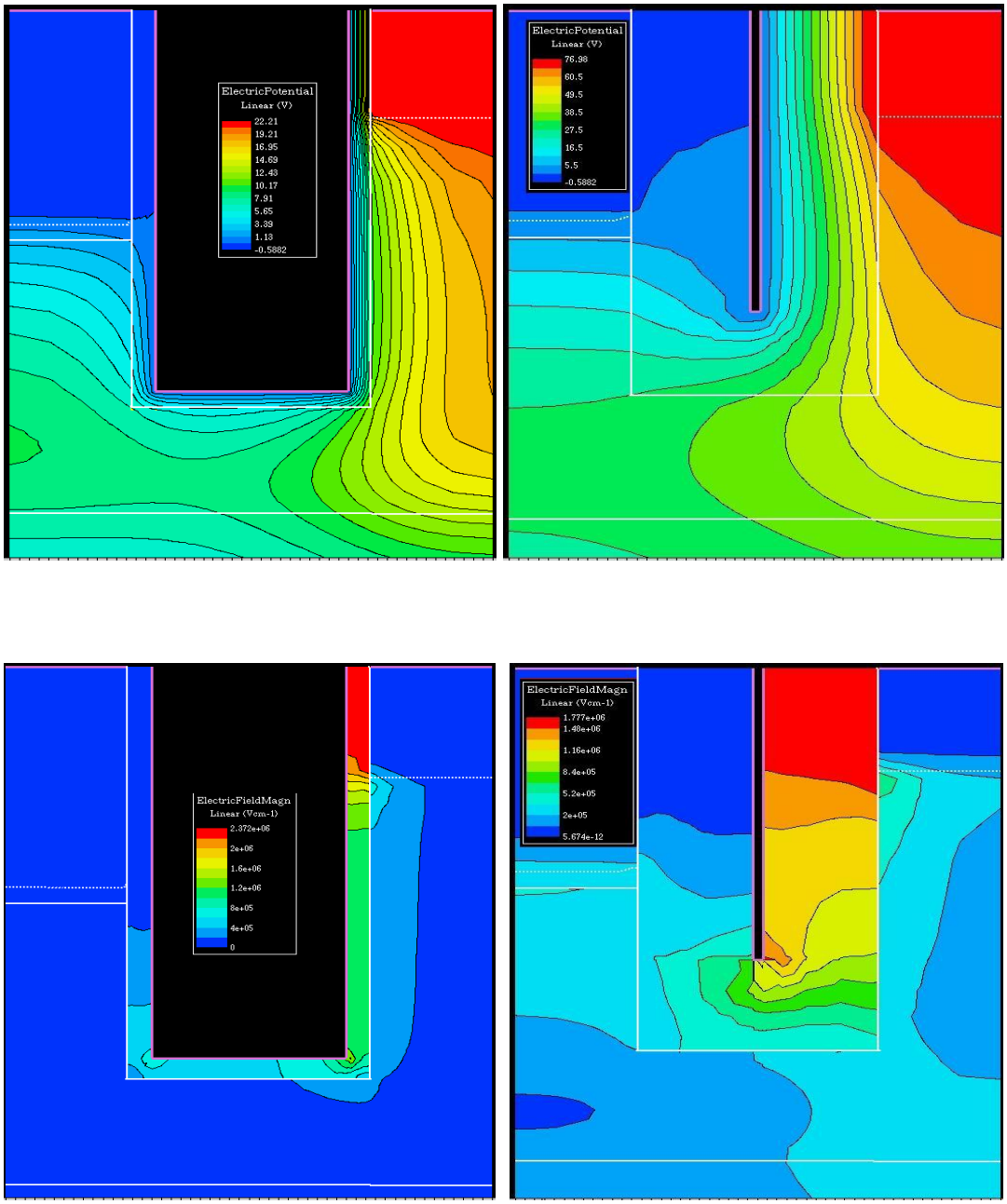

Fig. 5.3: Potential (upper) and electrical field (lower) distribution in the hybrid diode for Ndrift=2E16 cm $^{-3}$ and different oxide thickness: Tox=0.1microns (left) and 0.48 microns (right).

For N drift = 5e16 cm^{-3} (see Fig. 5.4), one can see that the drift region is only partially depleted and the field plate action is insufficient. The potential is distributed only under the P-body/N-drift junction on the left handside of the trench and the critical electrical field is reached at this junction, which causes the breakdown.

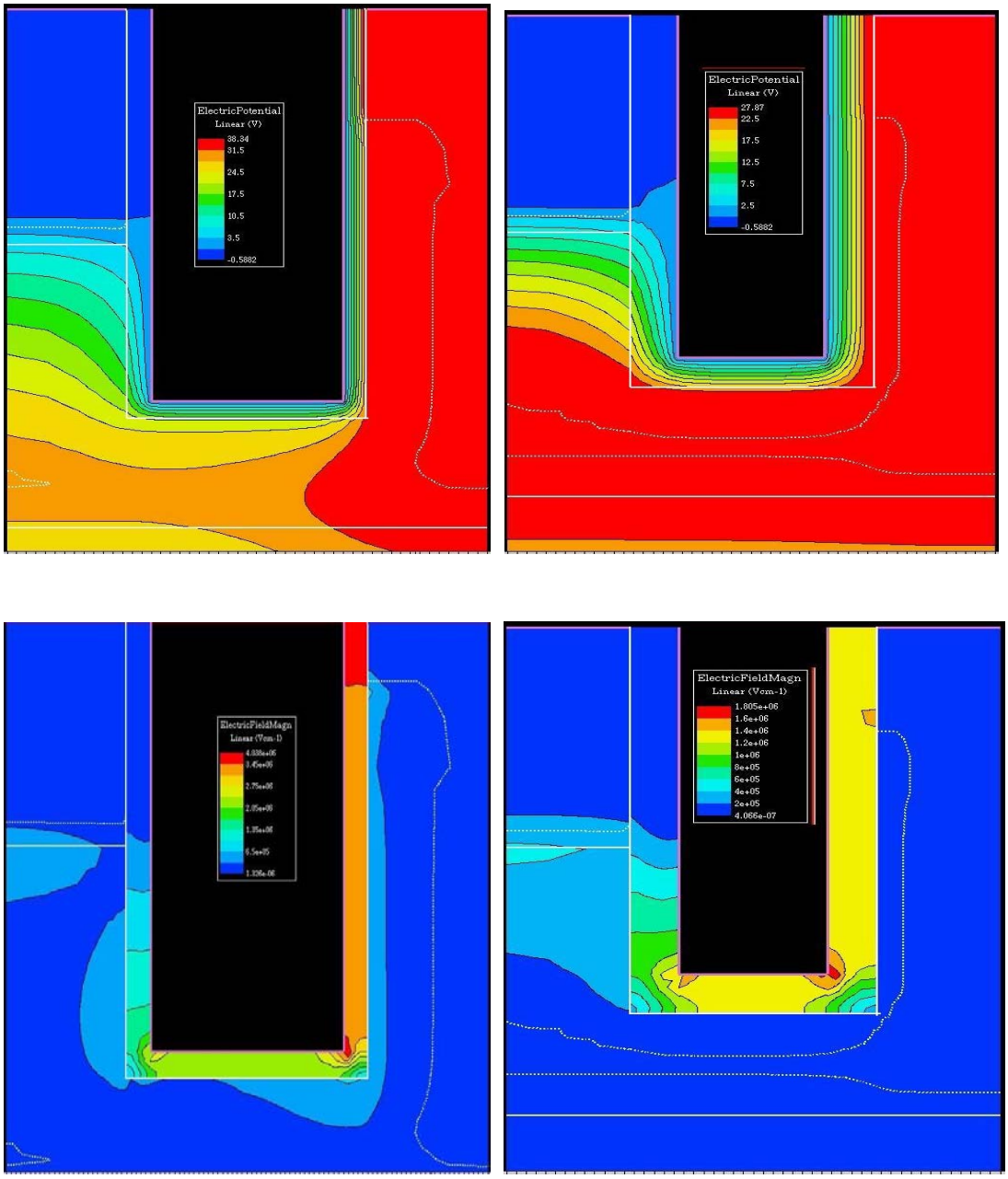

Fig. 5.4: Potential (upper) and electrical (lower) distribution in the hybrid diode for N drift =5E16 cm $^{-3}$ and different oxide thickness: Tox=0.1 microns (left) and 0.2 microns (right)

5.4 Hybrid Diode for 50 V domain

In this section the hybrid diode device optimized for 50V will be discussed. The optimal values leading to the most compact 50 V hybrid diode are listed in Table 5.2. Providing the optimal oxide thickness of 0.3 μm, the trench width can actually be further reduced.

Table 5.2: Optimized hybrid diode parameters (50V)

Optimized diode parameters	Values
Trench width	0.8 μm
Trench depth	1.0 μm
Oxide thickness	0.3 μm
Actual width	1.0 μm
Thickness below Trench	0.5 μm
Body depth	0.3 μm
N- (drift region) doping	2E16 cm^{-3}
P- (body) doping	1E18 cm^{-3}
P substrate doping	3E15 cm^{-3}
Drift length	2.02 μm

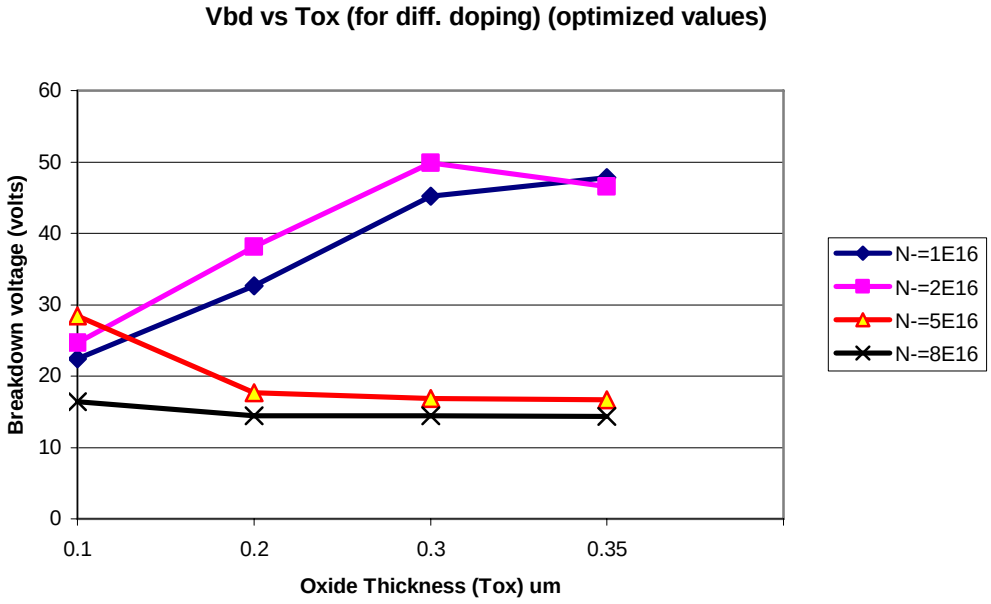

Fig. 5.5: Breakdown voltage vs. Oxide thickness.

An example of the optimization process is shown in Fig. 5.5, where breakdown voltage is plotted as a function of oxide thickness. The optimal oxide thickness of 0.3 μm is clearly observed. Finally, Fig. 5.6 shows potential and electrical field distribution in the optimized 50 V hybrid diode. The potential is almost linearly distributed along all three sides of the trench and the highest electrical fields are observed at the P-body/N-drift junction and under the drain.

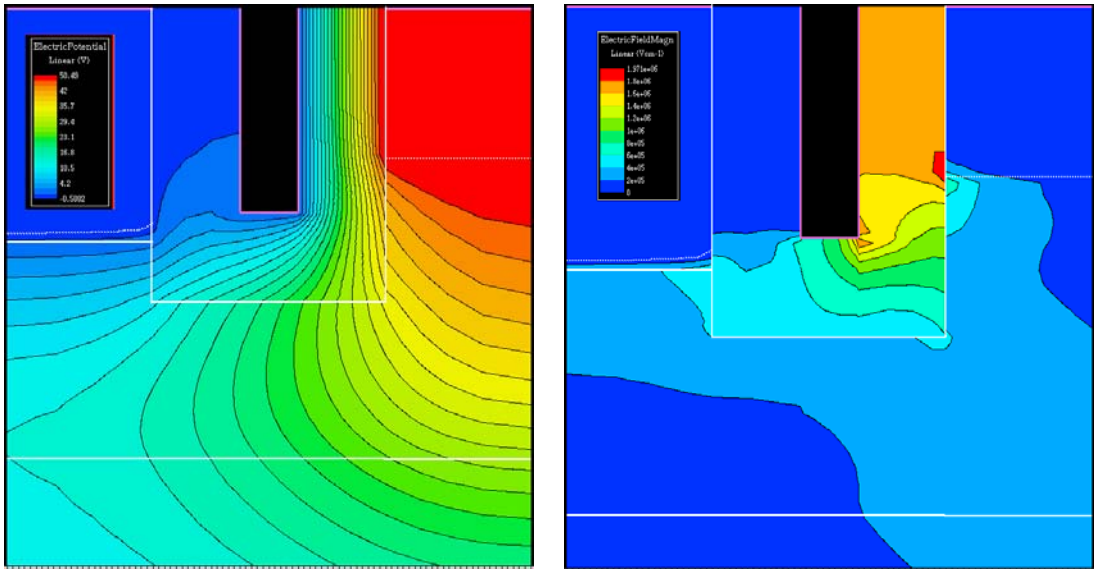

Fig. 5.6: Potential and Electrical field distribution for 50V.

5.5 Hybrid Diode for 100 V domain

In this section the hybrid diode device optimized for 100V is discussed. The optimized values of design parameters for 100 V operations are listed in Table 5.3. Providing the optimal oxide thickness of 0.8 μm, the trench width can actually be further reduced.

Table 5.3: Optimized hybrid diode parameters (100V)

Optimized diode parameters	Values
Trench width	2.1 μm
Trench depth	2.1 μm
Oxide thickness	0.8 μm
Actual width	1.0 μm
Thickness below trench	0.5 μm
Body depth	0.8 μm
N- (drift region) doping	2E16 cm^{-3}
P- (body) doping	1E18 cm^{-3}
P substrate doping	3E15 cm^{-3}
Drift length	4.94 μm

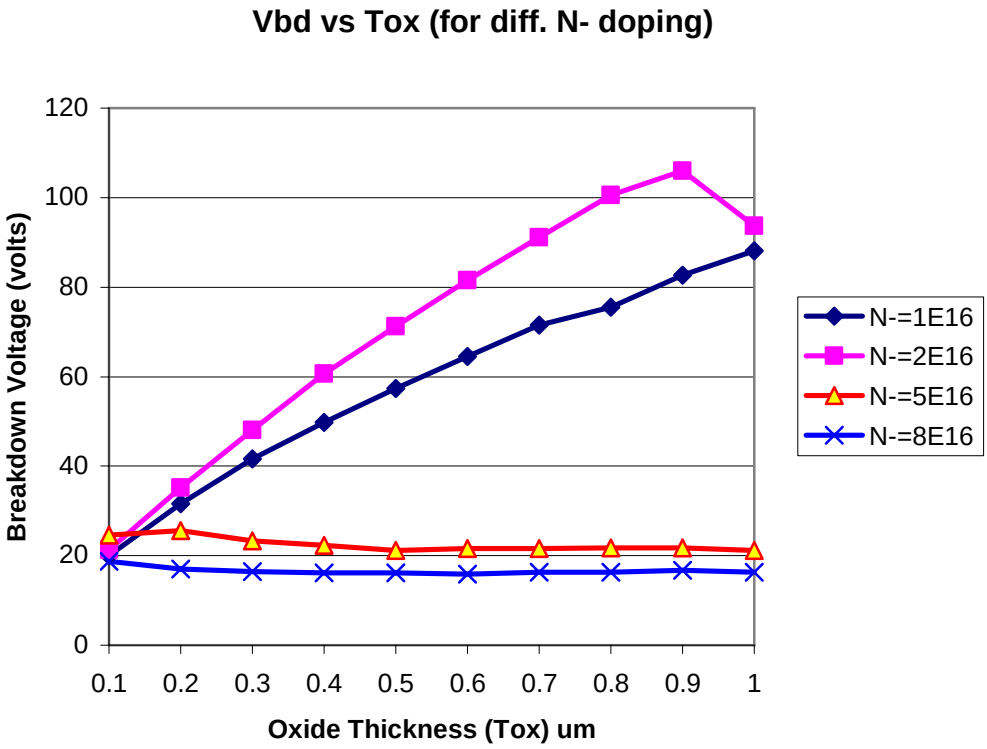

Fig. 5.7: Breakdown voltage vs. Oxide thickness.

An example of the optimization process is shown in Fig. 5.7, where breakdown voltage is plotted as a function of oxide thickness. The optimal oxide thickness of 0.8-0.9 μm is clearly observed. Finally, Fig. 5.8 shows potential and electrical field distribution in the optimized 100 V hybrid diode. The potential is almost uniformly distributed along all three sides of the trench and the highest electrical fields are under the drain.

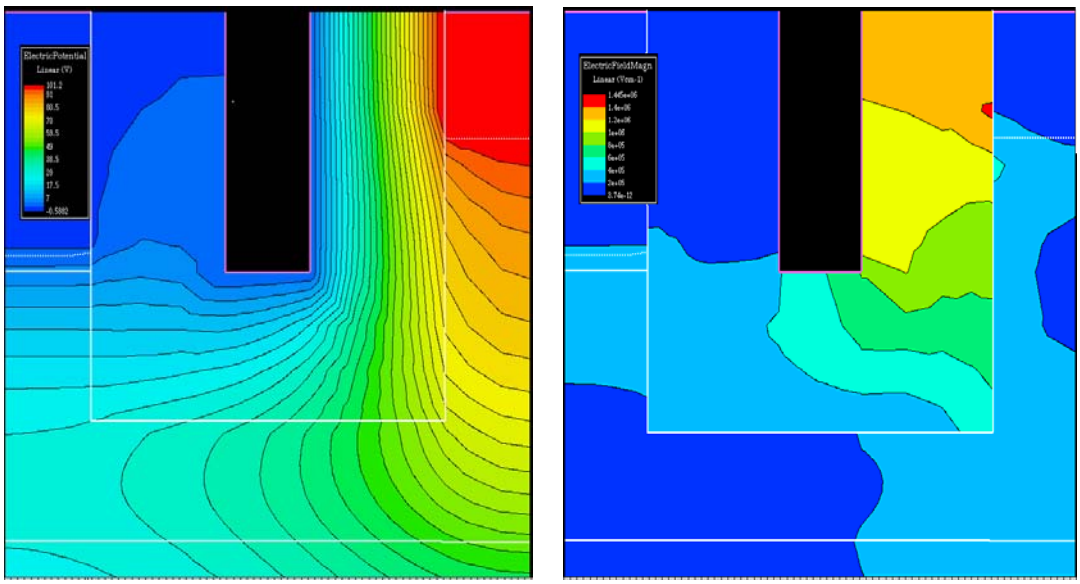

Fig. 5.8: Potential and Electrical field distributions for 100V.

5.6 Conclusion

A simple hybrid diode was simulated and the influence of different parameters on the breakdown voltage was studied. The studied parameters were trench width, trench depth, oxide thickness, drift length and doping concentration. The device was optimized for 50V and 100V operations. Here the optimal doping concentration value was found to be 2E16 cm^{-3} and optimal oxide thickness of 0.3 μm (50V) and 0.8μm (100V) was found.

CHAPTER 6 HYBRID TRANSISTOR

6.1 Introduction

As the future power integrated circuits for power management and automotive electronics requires integration of power electronic components into advanced CMOS technology processes, a novel hybrid transistor is analyzed in this chapter. The hybrid transistor is based on the hybrid diode discussed in the previous chapter. It further includes gate and source region. The design parameters optimized for the hybrid diode for 50 V and 100 V operations were used for the simulations of the hybrid N-channel transistor. It was verified that the hybrid transistor and hybrid diode exhibit essentially identical breakdown voltages for identical design parameters. Furthermore, the hybrid transistor was optimized for a threshold voltage of 1 V and a specific on-resistance was determined. The best values of $BV_{DS} - R_{on,sp}$ for hybrid transistor were benchmarked against the state-of-the-art lateral integrated transistors.

6.2 The simulated Structure

Fig. 6.1 shows the two dimensional view of the hybrid transistor simulated using the MEDICI simulator. The source, drain, gate, field plate and body contacts are on the top surface of the device. This device consists of a vertical trench with a field plate insulated from the drift region by a thick oxide (Tox). In the subtrench on the left handside of the original trench is located gate, which is separated from the transistor channel and from the field plate by a thin gate oxide (Tgox). The drain (N++) is located on the right-hand side, while source (N++) and body contact (P++) are located on the left-hand side. The source and body are sharing a common electrode. The N-drift region stretches along the trench sidewalls and the P body region is located in the upper left handside and aligned in depth with the gate. The breakdown voltage was simulated for different values of trench width, trench depth, drift length, oxide thickness, thickness below trench and doping concentration.

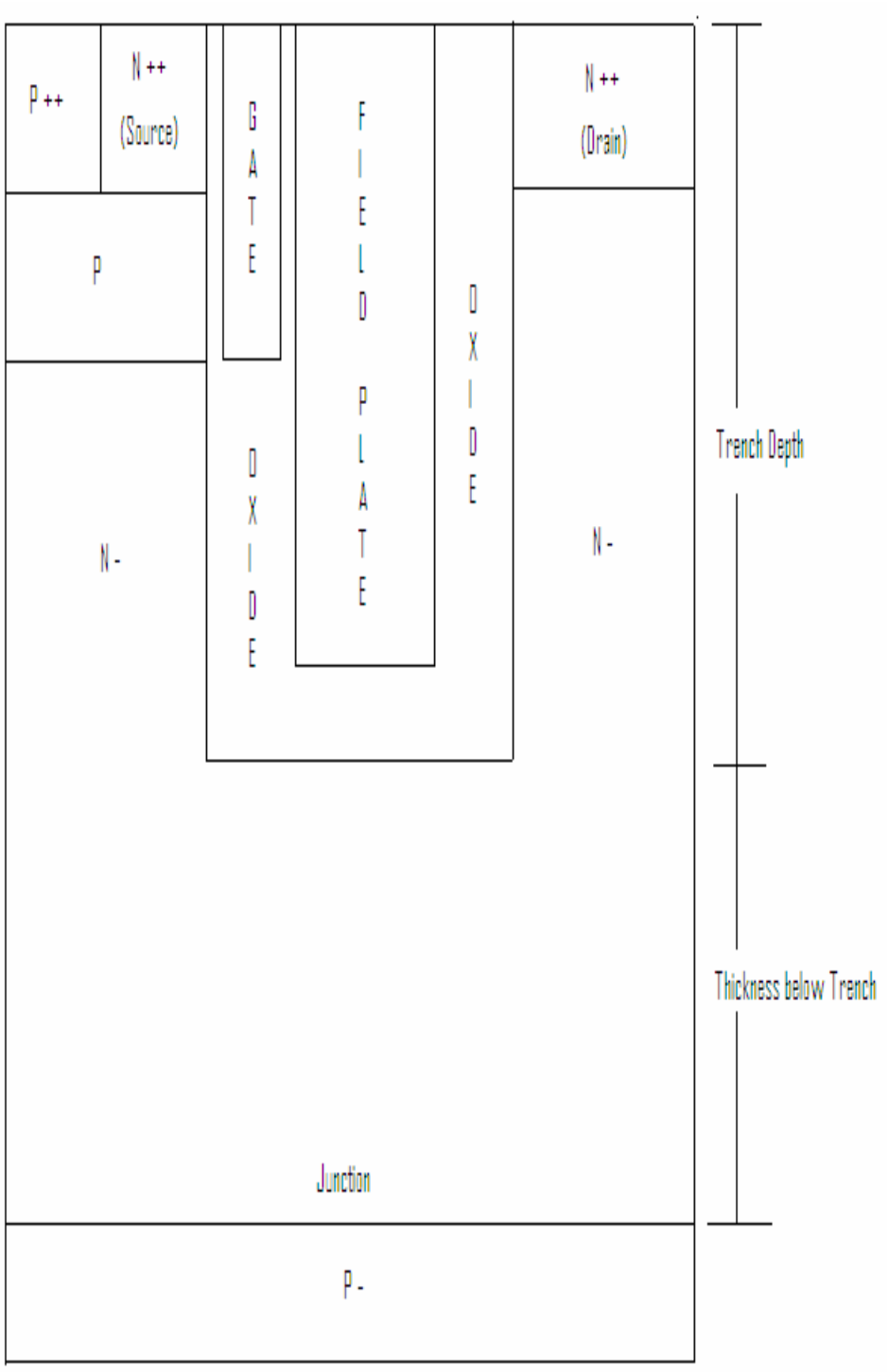

Fig. 6.1: Hybrid NMOS Transistor schematic.

6.3 Simulation Results and Analysis

6.3.1 50V Hybrid transistor: off-state characteristics

The trends in breakdown voltage dependence on the device parameters simulated for hybrid diode for 50 V domain were verified also for the hybrid NMOS transistor. Fig. 6.2 shows the breakdown voltage as a function of doping concentration. One can see a clear optimum for a Ndrift = 2e16 cm^{-3}. Providing the drift region width of 1 micron, the optimal doping dose of the drift region is 2e12 cm^{-2}. This corresponds very well with the ideal double-sided RESURF dose (mirrored stripe configuration).

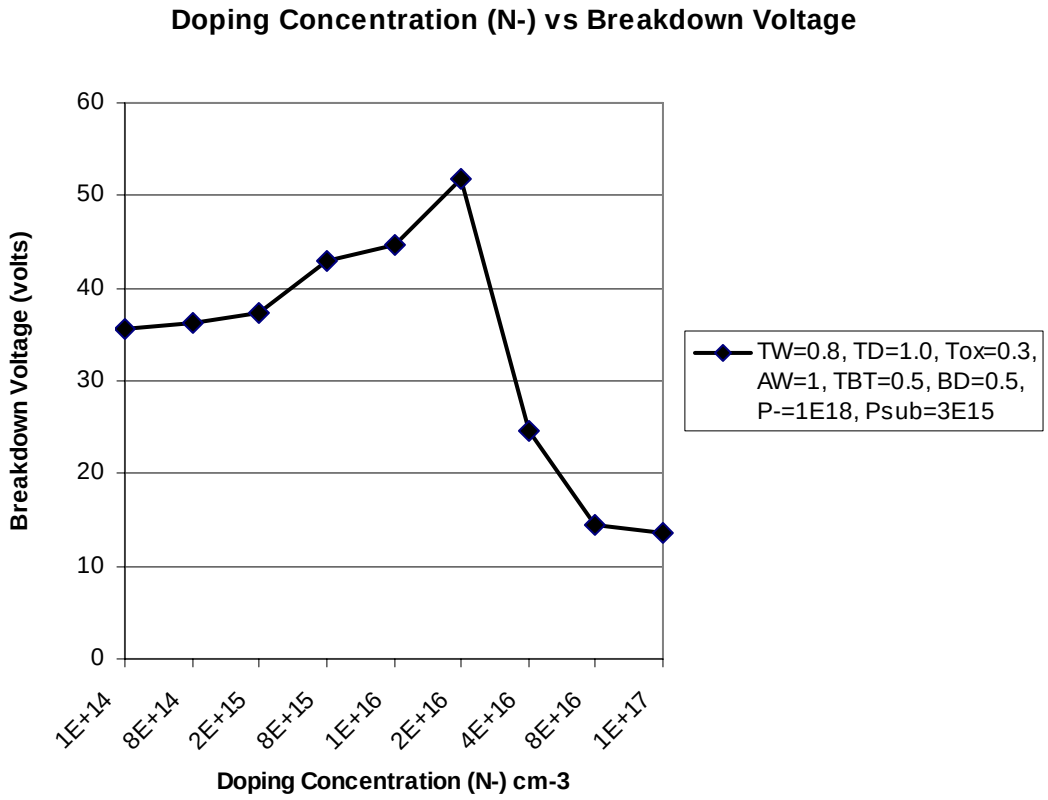

Fig. 6.2: Breakdown voltage vs. Doping concentration.

Fig. 6.3 shows breakdown voltage as a function of oxide thickness Tox. For an optimal drift region doping concentration, the highest breakdown voltage is achieved for Tox=0.3 μm. For Tox larger than 0.3μm, the field plate influence reduces due to weaker capacitive coupling. The optimal design parameters for hybrid NMOS transistor for 50 V domain are summarized in Table 6.1. The simulated potential and electrical field distributions of the optimal 50 V hybrid NMOS transistor are shown in Fig. 6.4.

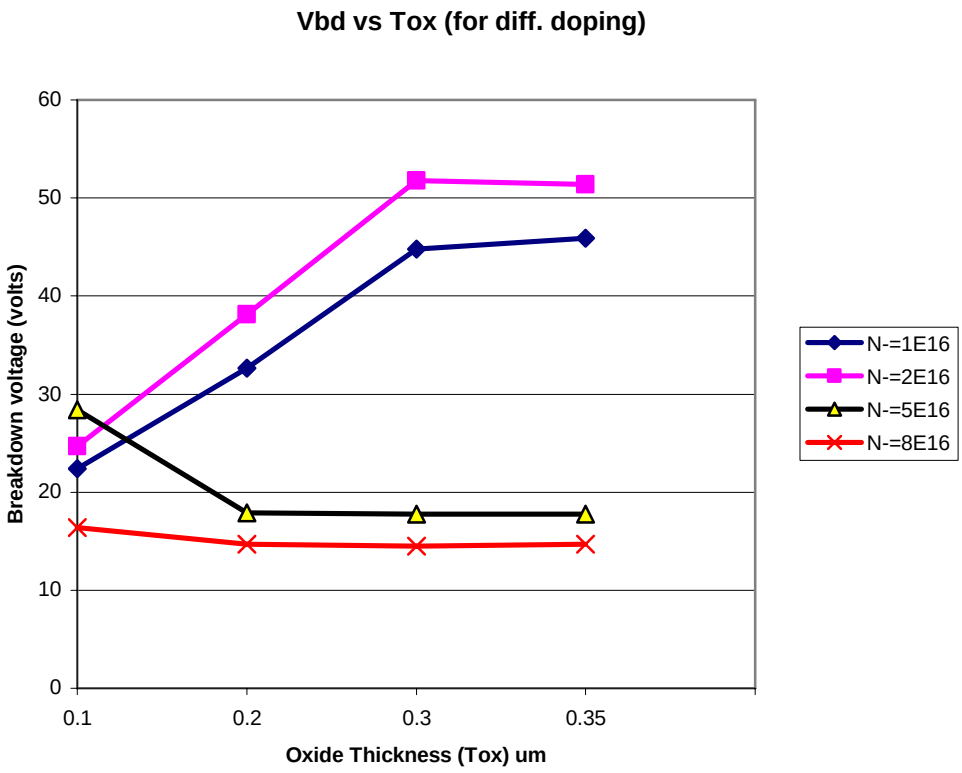

Fig. 6.3: Breakdown voltage vs. Oxide thickness.

Table 6.1: Optimal parameters for 50V hybrid NMOS transistor

Transistor Parameters (50V)	Values
Trench width	0.8 μm
Trench depth	1.0 μm
Oxide thickness	0.3 μm
Actual width	1.0 μm
Thickness below Trench	0.5 μm
Body depth	0.3 μm
N++/P++	0.5 μm
Gate oxide	0.010 μm
N- (drift) doping	2E16 cm^{-3}
P- doping	1E18 cm^{-3}
P substrate doping	3E15 cm^{-3}

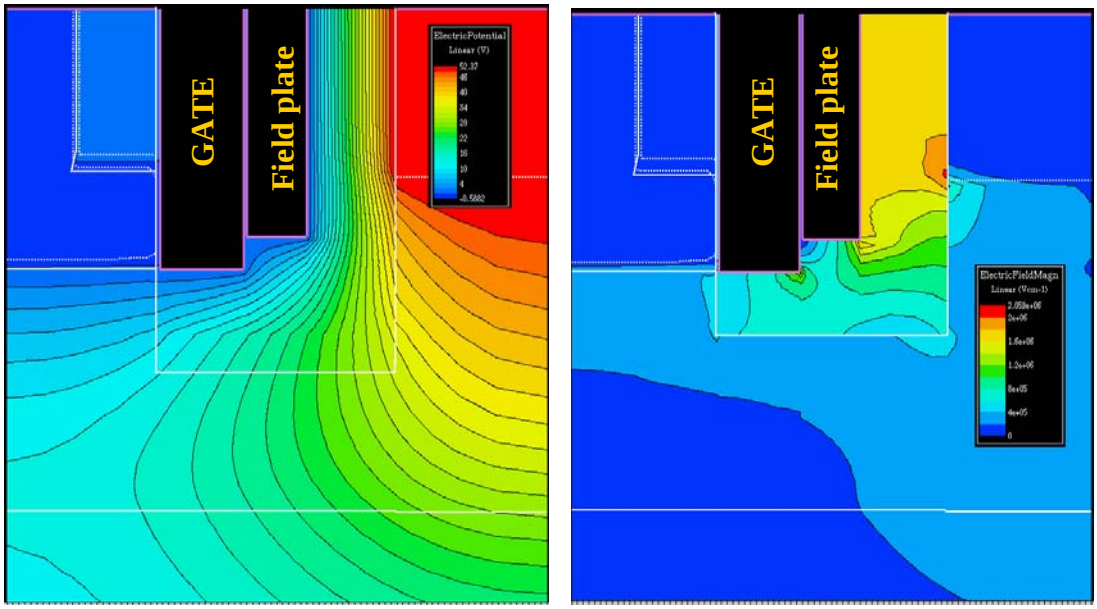

Fig. 6.4: Potential and Electrical field distributions for optimized 50V hybrid NMOS transistor.

6.3.2 50 V Hybrid transistor: on-state characteristics

As a basic on-state characteristic, a drain current as a function of gate voltage was simulated. Fig. 6.5 shows the Id -Vg curve for a drain voltage of 0.05 V. The body doping was 6.7E17 cm^{-3} and it was chosen to achieve a threshold voltage of 1 V. The simulated current allows us to determine the specific on-resistance. We found a specific on-resistance of Ron,sp = 21.7 $m\Omega.mm^2$ for Vg=5V.

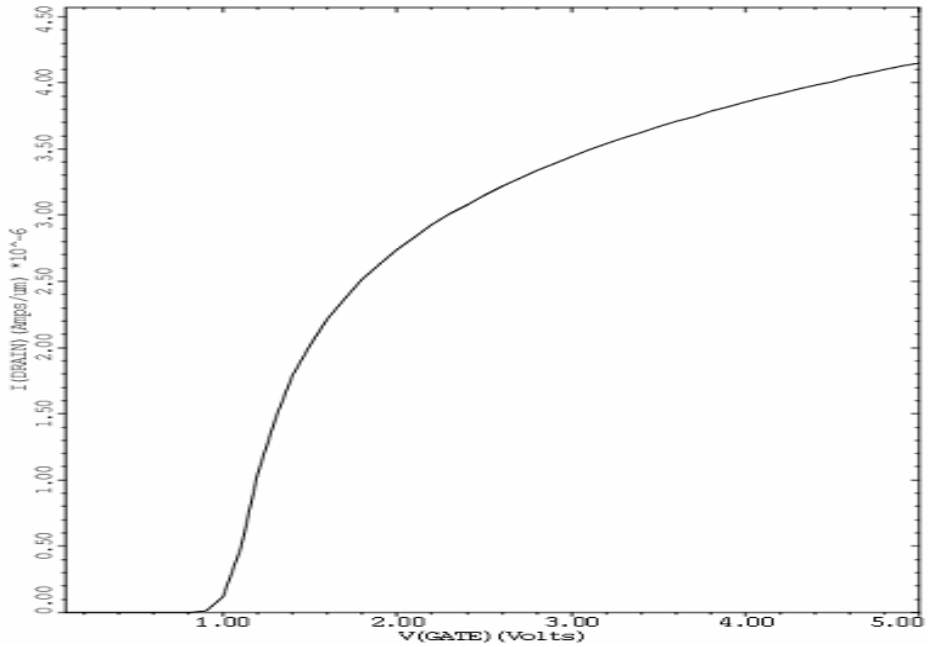

Fig. 6.5: Id-Vg graph for Pwell=6.7E17 cm^{-3}, Vt=1V, 50V.

6.3.3 100V Hybrid transistor: off-state characteristics

The breakdown voltage as a function of drift region doping concentration and oxide thickness doping are shown in Fig. 6.6 and 6.7, respectively. The optimal doping concentration is again 2e16 cm^{-3} and an optimal oxide thickness is 0.8 microns. The optimal parameters for 100 V NMOS device are summarized in Table 6.2.

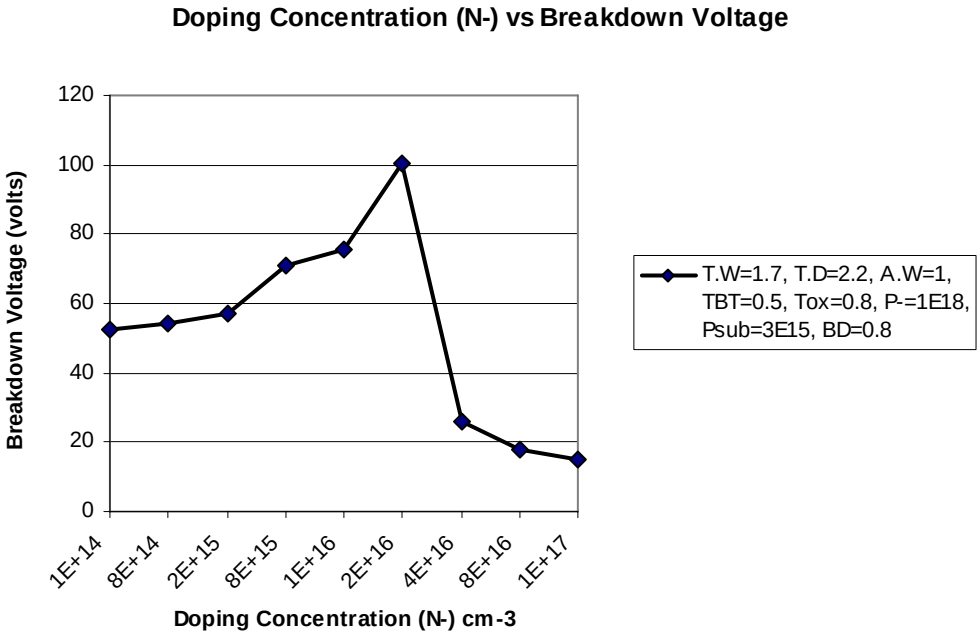

Fig. 6.6: Breakdown voltage vs. Doping concentration.

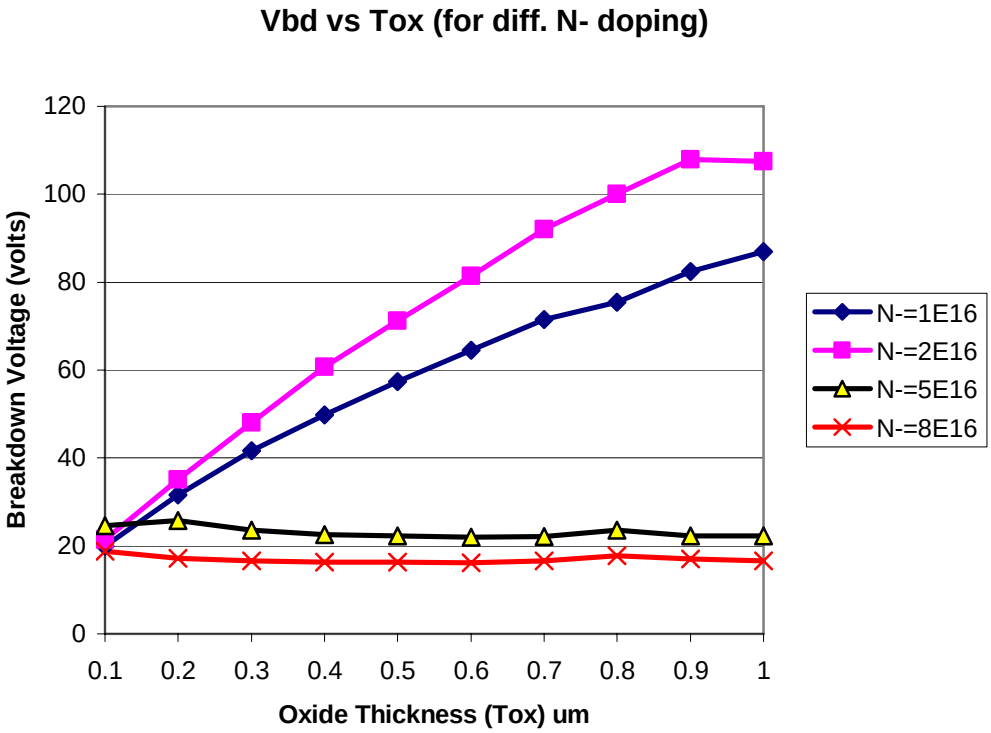

Fig. 6.7: Breakdown voltage vs. Oxide thickness.

Table 6.2: Optimal parameters for 100V hybrid NMOS transistor

Transistor Parameters (100V)	Values
Trench width	1.7 μm
Trench depth	2.2 μm
Oxide thickness	0.8 μm
Actual width	1.0 μm
Thickness below Trench	0.5 μm
Body Depth	0.8 μm
N++/P++	0.5 μm
Gate oxide	0.010 μm
N- (drift) doping	2E16 cm^{-3}
P- doping	1E18 cm^{-3}
P substrate doping	3E15 cm^{-3}

The potential and electric field distribution for the optimized 100 V hybrid NMOS transistor are shown in Fig. 6.8. The potential distribution is nearly ideal linear in the drift region around the whole trench. The voltage handling capability is limited by the high electrical field under the drain.

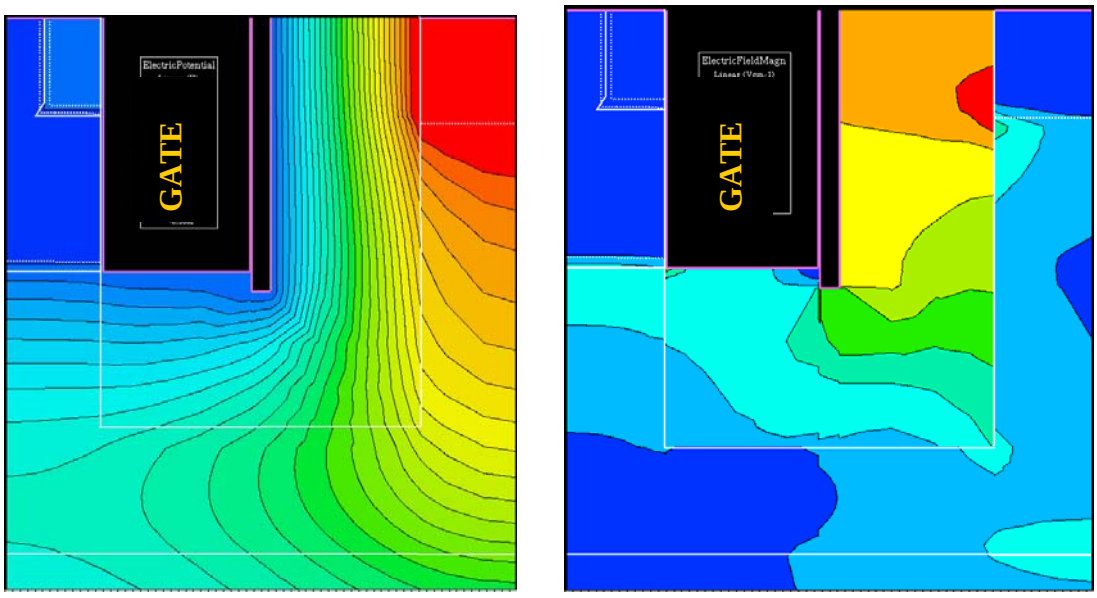

Fig. 6.8: Potential and Electrical field distribution for optimized 100V hybrid NMOS Transistor.

6.3.4 100 V Hybrid transistor: on-state Characteristics

The drain current versus gate voltage was simulated for the optimized 100 V hybrid NMOS transistor and Id-Vg curve for Vd = 0.05 V is shown in Fig. 6.9. The threshold voltage is approximately 1 V. We have determined a specific on-resistance of 76.7 $m\Omega mm^2$.

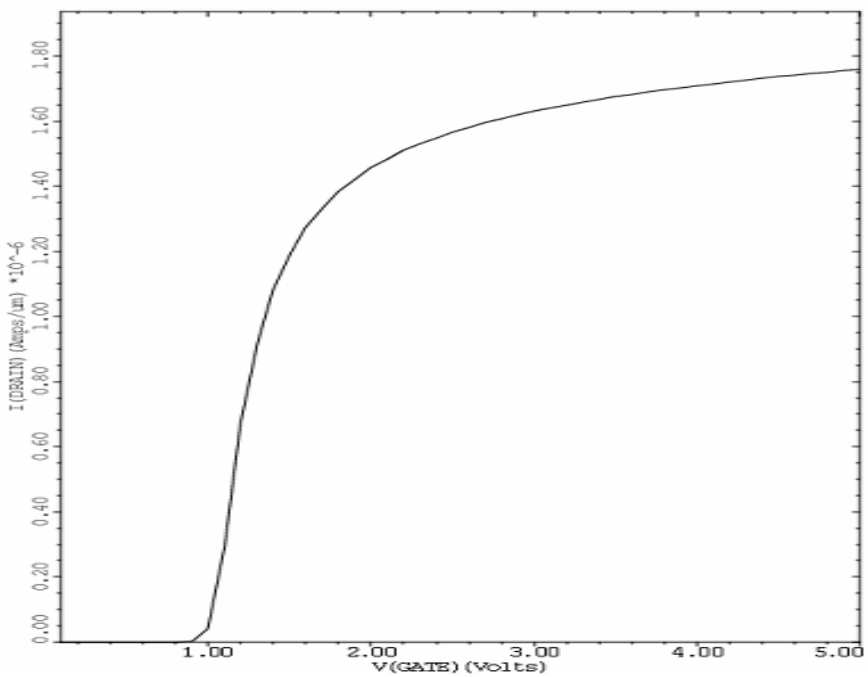

Fig. 6.9: Id-Vg graph for Pwell=4.4E17 cm^{-3}, Vt=1V, 100V.

6.4 Benchmarking

The studied hybrid NMOS transistor optimized for 50V and 100V was compared with current best-in-class lateral BCD technologies in Fig. 6.10. The simulated hybrid NMOS features Ron,sp = 21.7 mΩmm^2 for 50V and Ron,sp=76.7 mΩmm^2 for a 100V domain, respectively. The hybrid transistor outperforms significantly all existing solutions.

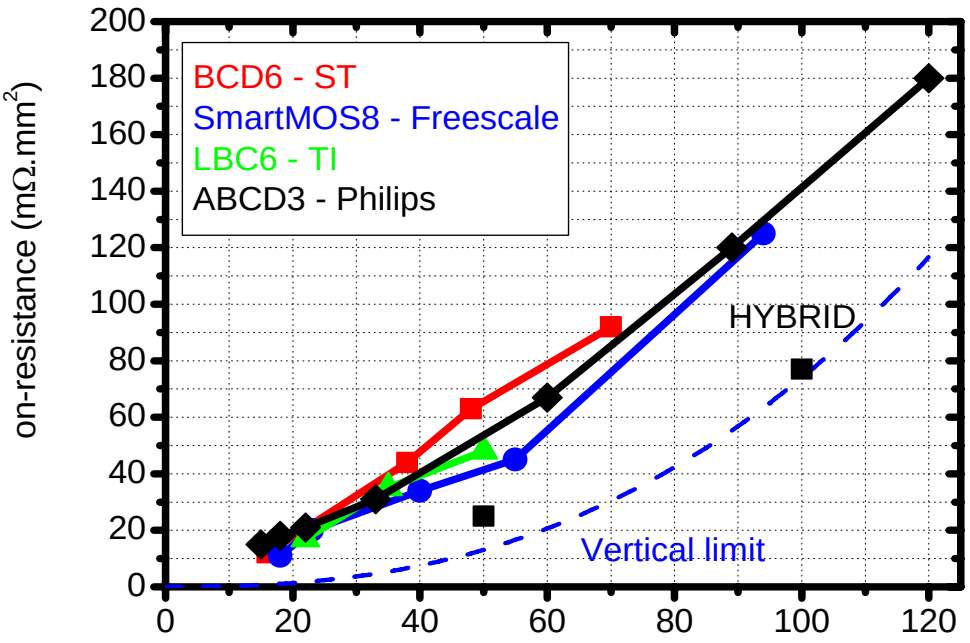

Fig. 6.10: Comparison of Ron,sp - BVds trade-off for hybrid transistor and existing BCD technologies

CHAPTER 7 CONCLUSION

7.1 PRESENT WORK

In this work, a novel hybrid transistor for future power integrated circuits was proposed. This concept aims to enhance scaling of power transistors. The device was optimized for two different breakdown voltages (50V, 100V) and very good results were obtained from the simulation.

A specific on-resistance of 21.7 $m\Omega mm^2$ and 76.7 $m\Omega mm^2$ is obtained for 50 V and 100 V domain, respectively. This is significantly better than all existing BCD technologies.

7.2 FUTURE WORK

The possible work which can be carried out on this project in the future is by further optimizing the device for 25V, 75V, 125V and 150V respectively by altering the parameters discussed in this work. Therefore this device can be used for all sort of low voltage applications. It can also become the key component in all power integrated circuits.

LIST OF ABBREVIATIONS

ABCD – **Advanced BiCMOS DMOS**

BCD – **BiCMOS DMOS**

CMOS – **Complementary Metal Oxide Semiconductor**

DMOS – **Double Diffused MOS**

IC – **Integrated Circuit**

JFET – **Junction Field Effect Transistor**

LDMOS – **Lateral Double diffused MOS**

MOSFET – **Metal Oxide Semiconductor Field Effect Transistor**

NMOS - **N-type MOS**

PIC – **Power Integrated Circuits**

PMOS - **P-type MOS**

PN – **P-type and N-type junction**

RESURF – **Reduced Surface Field**

SOI – **Silicon on Insulator**

2D – **Two Dimensional**

LIST OF SYMBOLS

K - **Boltzmann's constant** ***(1.38 x 10^{-23} Joule/Kelvin)***

L - **Length** ***(m)***

N++ - **Highly doped N region** ***(cm^{-3})***

N - - **Lightly doped N region** ***(cm^{-3})***

Nd – **Doping Concentration** ***(cm^{-3})***

P++ - **Highly doped P region** ***(cm^{-3})***

P - - **Lightly doped P region** ***(cm^{-3})***

q- **Electronic charge** ***(1.602 x 10^{-19} Coulomb)***

R – **Resistance** ***(ohm)***

Rds, on – **on state drain source resistance** ***($m\Omega.mm^2$)***

Rsp – **Specific on-resistance** ***($m\Omega.mm^2$)***

Tox – **Oxide Thickness** ***(m)***

Ts – **Silicon thickness** ***(m)***

V- **Applied voltage** ***(volt)***

Vbd - **Breakdown Voltage** ***(volt)***

Vd - **Drain Voltage** ***(volt)***

Vg – **Gate Voltage (volt)**

Vt – **Threshold Voltage** ***(volt)***

W - **Width of the depletion layer** ***(m)***

x - **Spatial co-ordinate**

α **-** **Ionization coefficient**

$\in o$ **-** **Permittivity of vacuum** ***(8.854 x 10^{-12} Farad/meter)***

$\in si$ **-** **Dielectric constant of silicon (11.7)** ***(F/m)***

$\in ox$ **-** **Dielectric constant of oxide (3.8)** ***(F/m)***

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APPENDIX

A.I HYBRID NMOS DEVICE STRUCTURE

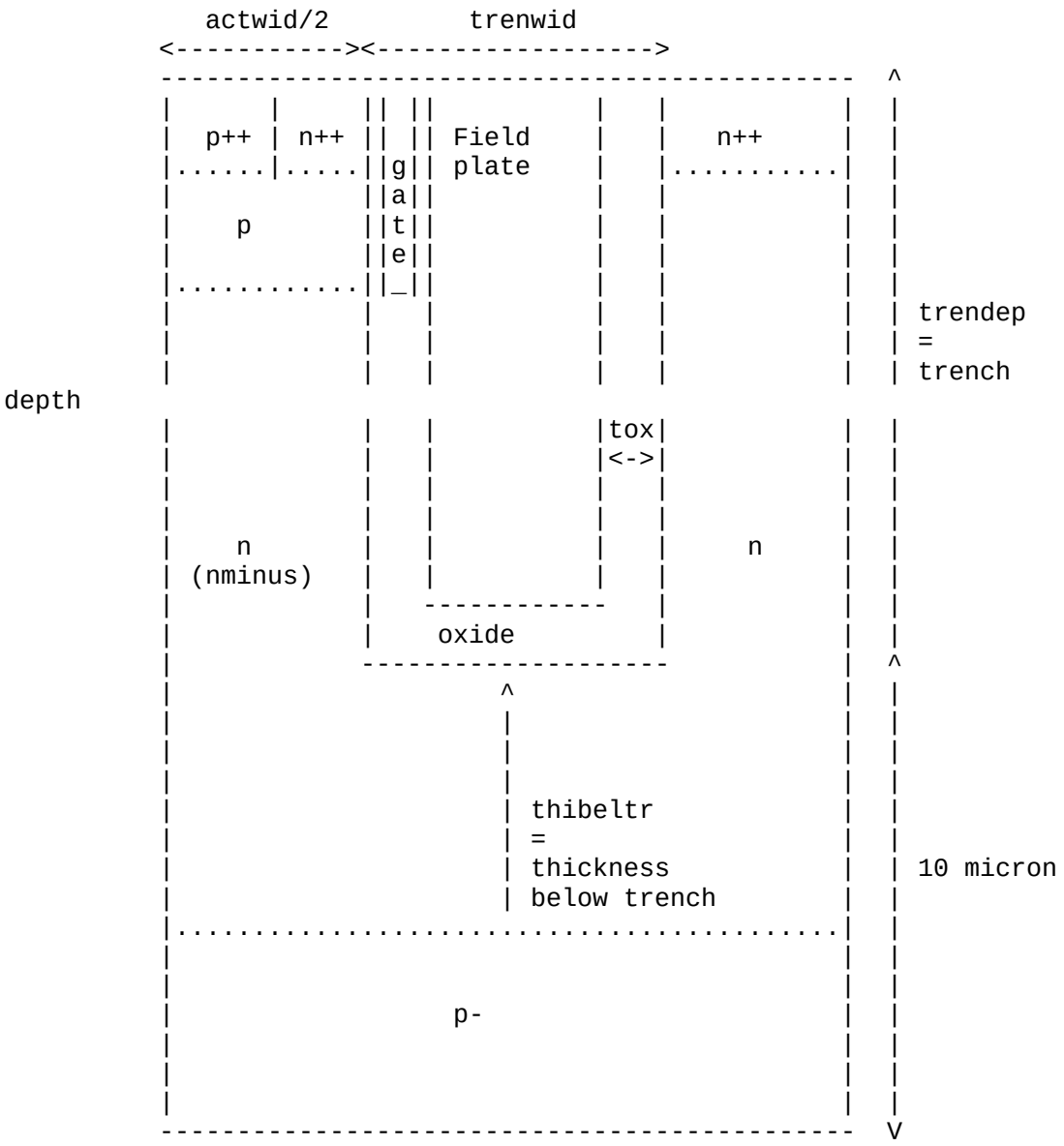

Fig. A.I.1 Hybrid NMOS Transistor Schematic.

A.II SIMULATION DATA

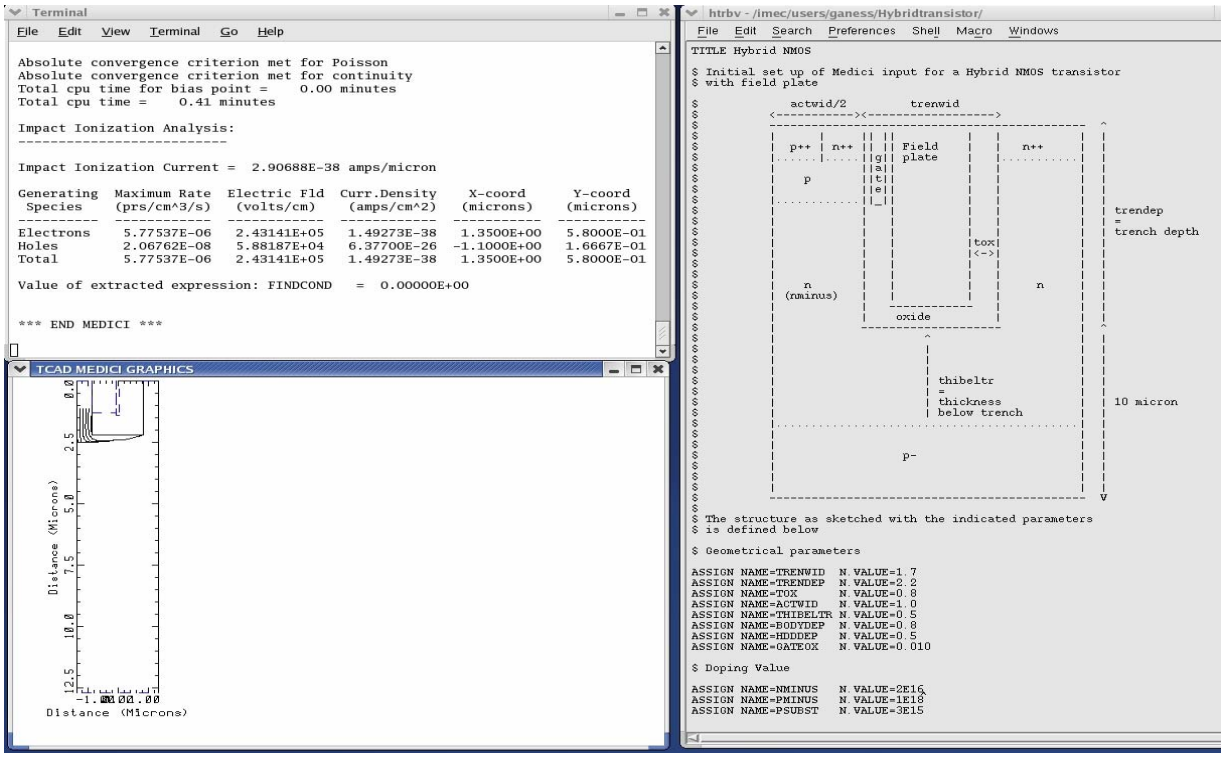

Fig. A.II.1 Simulation Window in LINUX

Fig. A.II.2 Taurus Visual 2D- Main Window

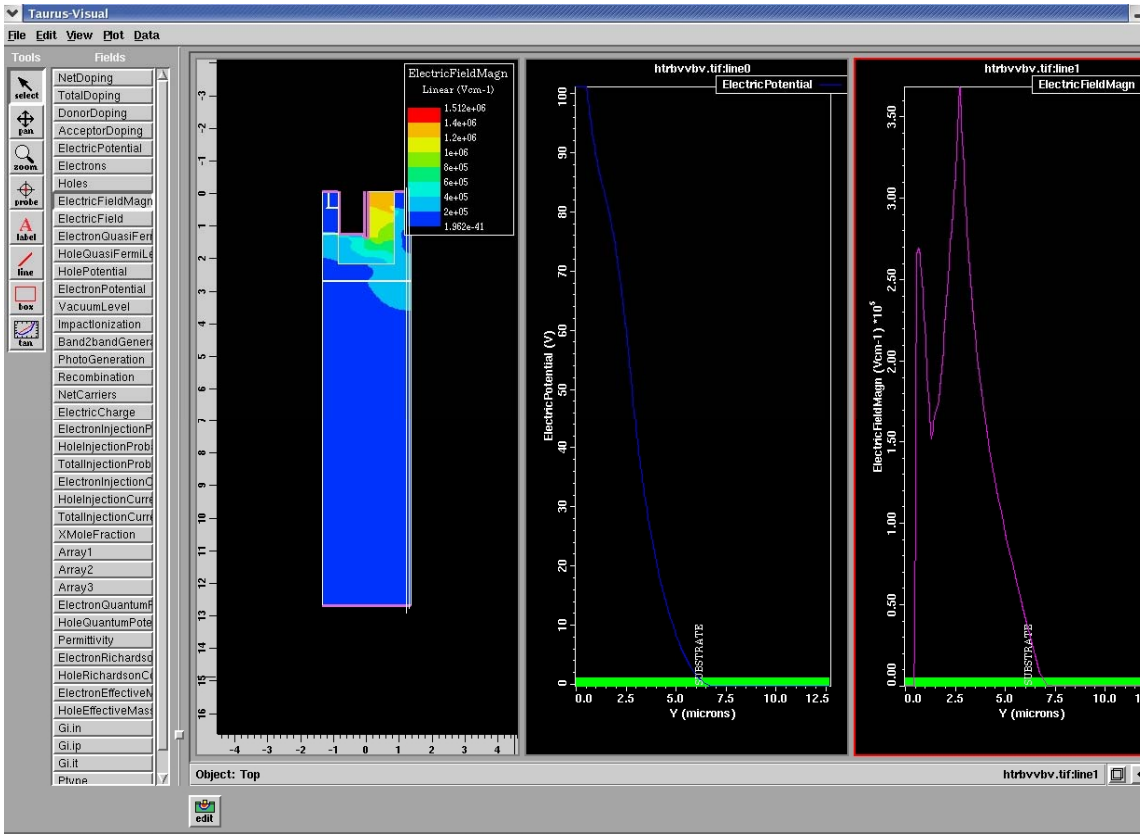

Fig. A.II.3 Taurus Visual 2D - Cut Curves Analysis

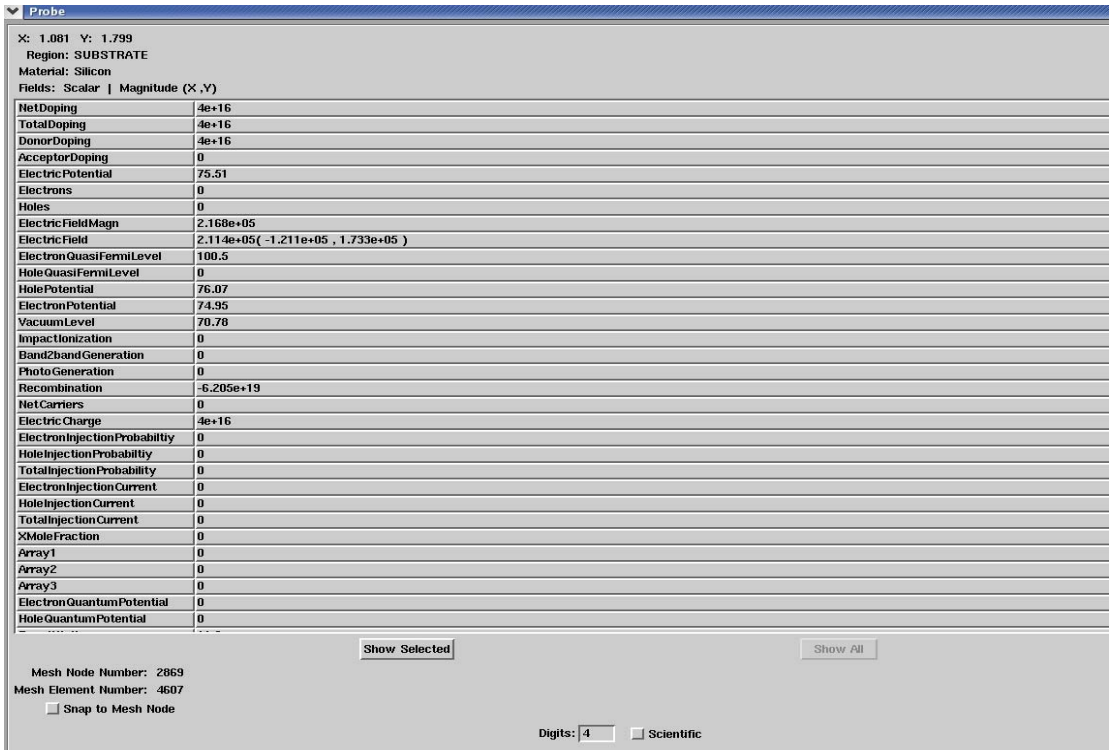

Fig. A.II.4 Taurus Visual 2D - Probe Values

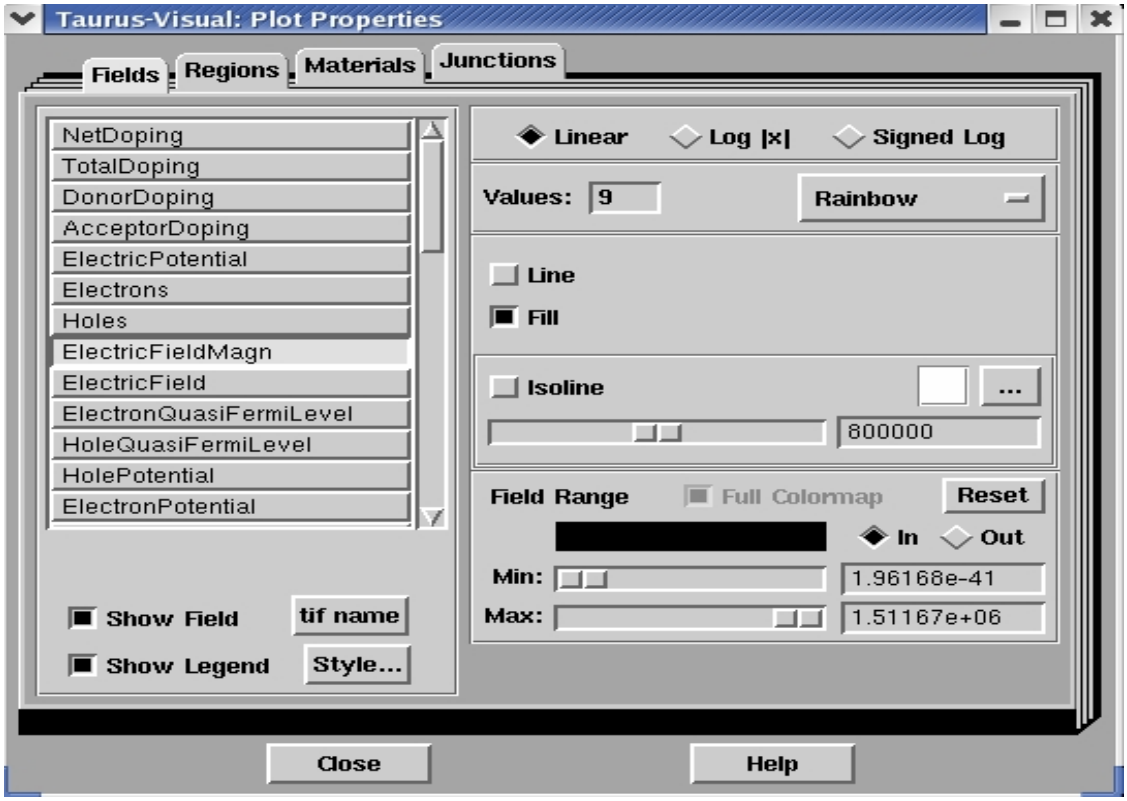

Fig. A.II.5 Taurus Visual 2D - Plot Properties - Fields

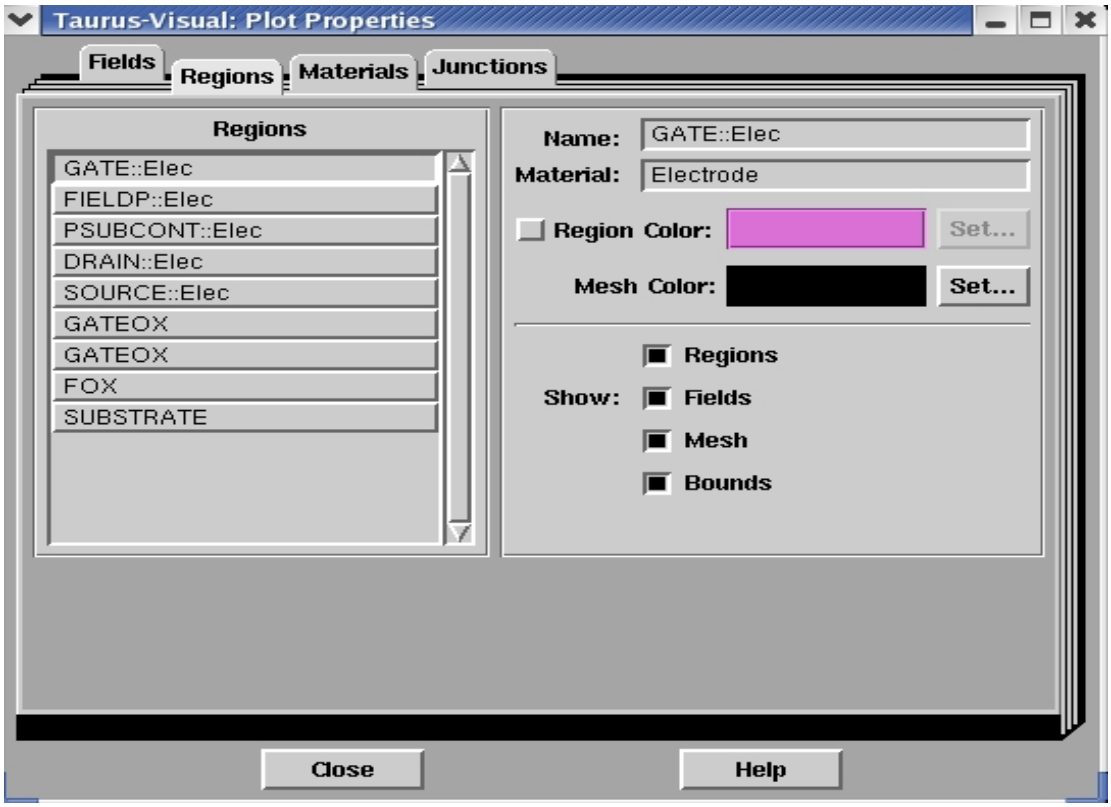

Fig. A.II.6 Taurus Visual 2D - Plot Properties - Regions

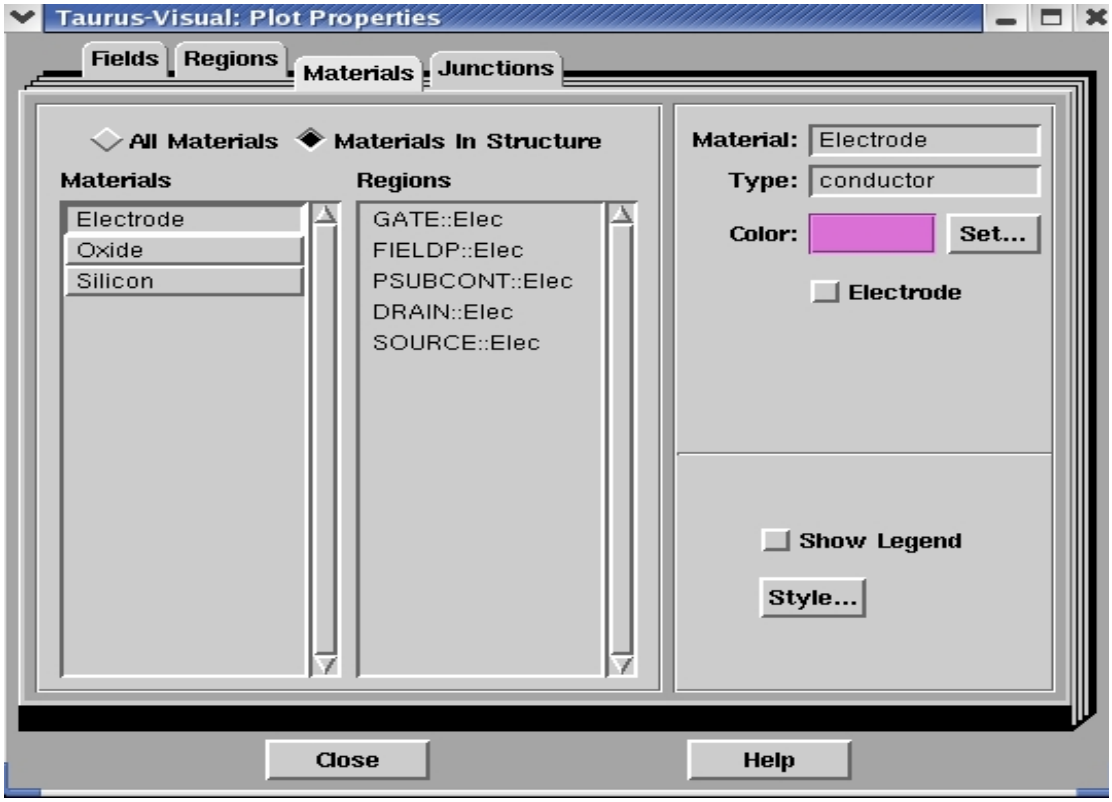

Fig. A.II.7 Taurus Visual 2D - Plot Properties - Materials

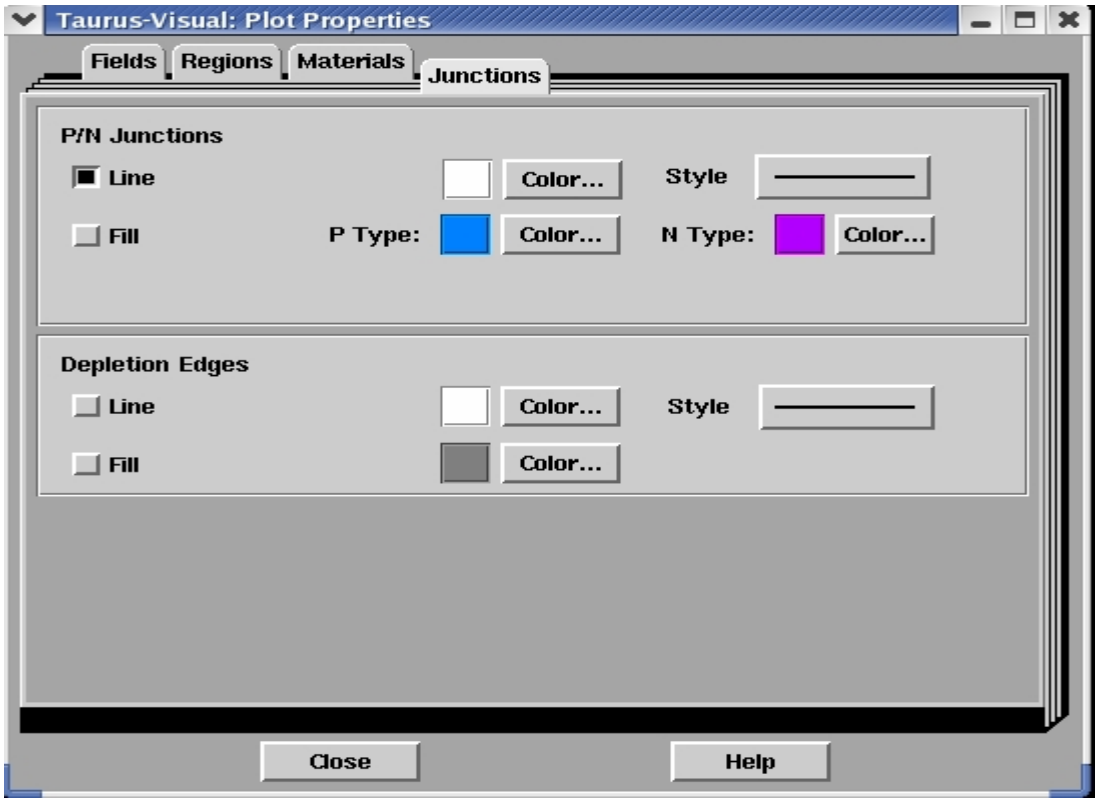

Fig. A.II.8 Taurus Visual 2D - Plot Properties – Junctions